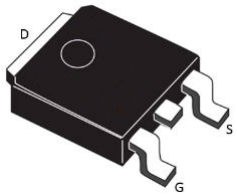
Silicon N-Channel Power MOSFET

V_{DSS}	200	V
I_D	5	A
P_D (T_C=25℃)	40	W
$R_{DS(ON)typ}$	0.5	Ω

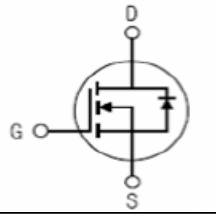
General Description:

HMR5N20 the silicon N-channel Enhanced VDMOSFETS, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-252, which accords with the RoHS standard.

TO-252



Inner Equivalent Principium Chart



Features:

- Fast Switching
- Low Gate Charge and Rdson
- Low Reverse transfer capacitances
- 100% Single Pulse avalanche energy Test

Applications:

- LED Lighting
- Charger
- Standby Power

Absolute (Tc=25℃ unless otherwise specified):

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	200	V
I_D	Continuous Drain Current	5	A
	Continuous Drain Current T_C = 100 °C	3.5	A
I_{DM} [a1]	Pulsed Drain Current	20	A
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS} [a2]	Single Pulse Avalanche Energy	150	mJ
dv/dt [a3]	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation	40	W
	Derating Factor above 25°C	0.6	W/℃
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, −55 to 150	℃
T_L	Maximum Temperature for Soldering	300	℃

Electrical Characteristics (Tc=25℃ unless otherwise specified):

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	200	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Bvdss Temperature Coefficient	ID=250uA,Reference25℃	--	0.21	--	V/℃
I_{DSS}	Drain to Source Leakage Current	V_{DS}=200V, V_{GS}=0V,T_a=25℃	--	--	1	μA
		V_{DS}=160V, V_{GS}=0V,T_a=125℃	--	--	100	
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS}=+30V	--	--	100	μA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS}=-30V	--	--	-100	μA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=2.5A	--	0.5	0.65	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1.0	1.7	2.5	V
Pulse width tp≤300μs,δ≤2%						

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}	Forward Transconductance	V_{DS}=25V,I_D=2.5A	--	2.0	--	S
C_{iss}	Input Capacitance	V_{GS}=0V,V_{DS}=25V f=1.0MHz	--	230	--	pF
C_{oss}	Output Capacitance		--	48	--	
C_{rss}	Reverse Transfer Capacitance		--	8	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	I_D=5A,V_{DD}=100V R_G=10Ω	--	6	--	ns
t_r	Rise Time		--	12	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	24	--	
t_f	Fall Time		--	11	--	
Q_g	Total Gate Charge	I_D=5A,V_{DD}=100V V_{GS}=10V	--	6.5	--	nC
Q_{gs}	Gate to Source Charge		--	2	--	
Q_{gd}	Gate to Drain (“Miller”)Charge		--	3	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)		--	--	5	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	40	A
V_{SD}	Diode Forward Voltage	I_S=5.0A,V_{GS}=0V	--	--	1.5	V
t_{rr}	Reverse Recovery Time	I_S=5.0A,T_j=25°C	--	103	--	ns
Q_{rr}	Reverse Recovery Charge	dI_F/dt=100A/us,	--	370	--	uC
I_{RRM}	Reverse Recovery Current	V_{GS}=0V	--	7.0	--	A
Pulse width tp≤300μs,δ≤2%						

Symbol	Parameter	Typ.	Units
$R_{\theta JC}$	Junction-to-Case	3.13	℃/W
$R_{\theta JA}$	Junction-to-Ambient	62.5	℃/W

[a1]: Repetitive rating; pulse width limited by maximum junction temperature

[a2]: L=10.0mH, I_D=5.5A, Start T_J=25℃

[a3]: I_{SD} =5A,di/dt ≤100A/us,V_{DD}≤BV_{DS}, Start T_J=25℃

Characteristics Curve:

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

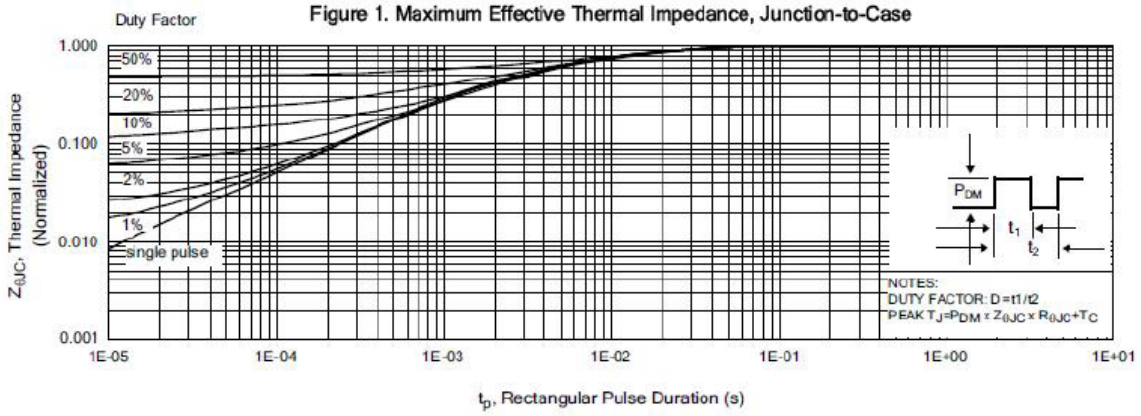


Figure 2. Maximum Power Dissipation vs Case Temperature

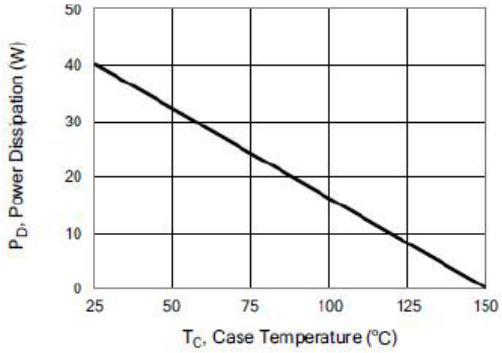


Figure3. Maximum Continuous Drain Current vs Case Temperature

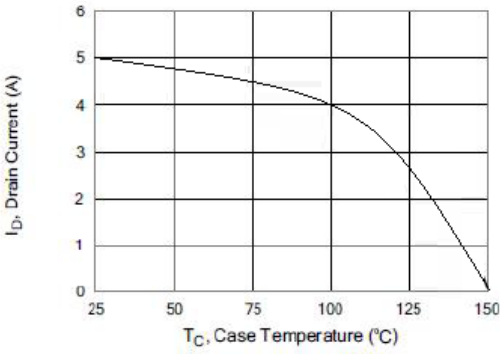


Figure 4. Typical Output Characteristics

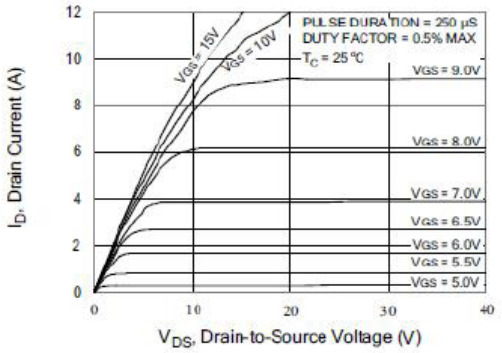


Figure5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current

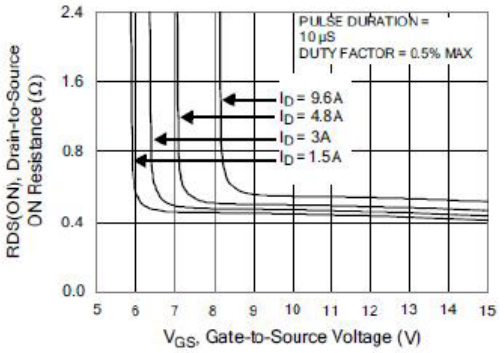


Figure 6. Maximum Peak Current Capability

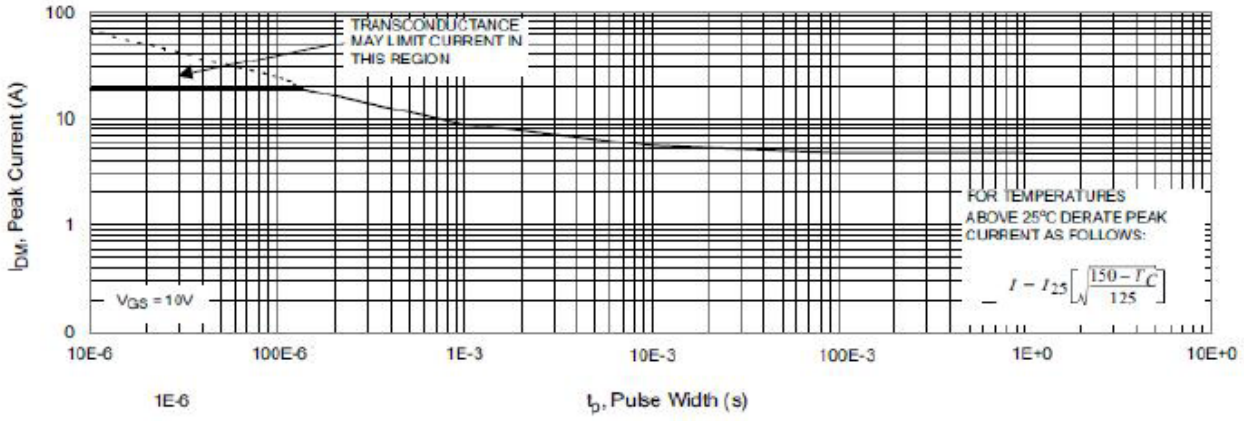


Figure 7. Typical Transfer Characteristics

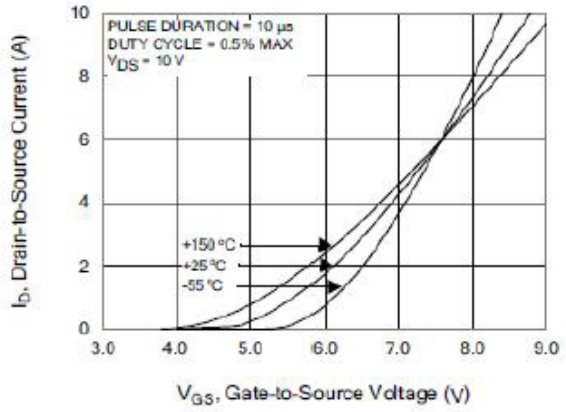


Figure 8. Unclamped Inductive Switching Capability

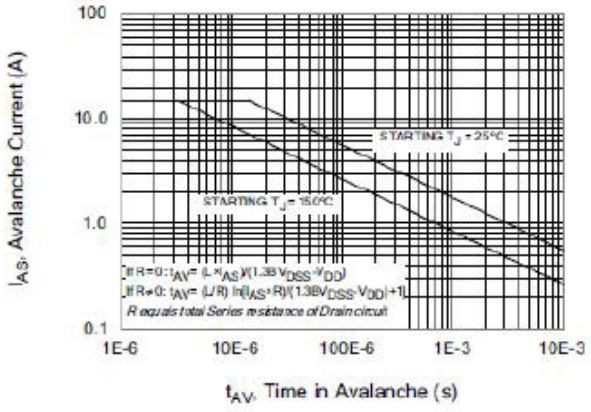


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

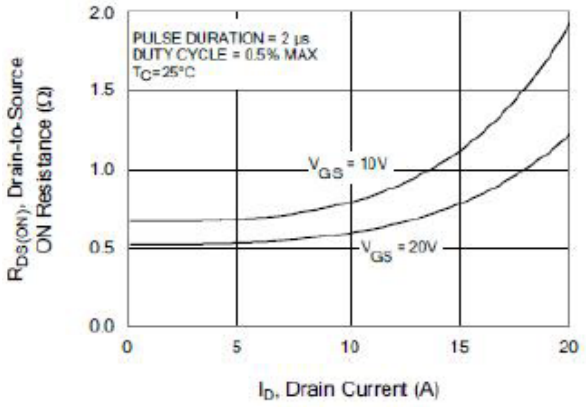


Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature

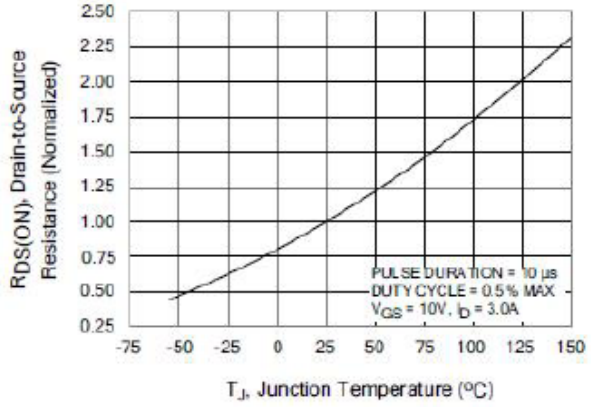


Figure 11. Typical Breakdown Voltage vs Junction Temperature

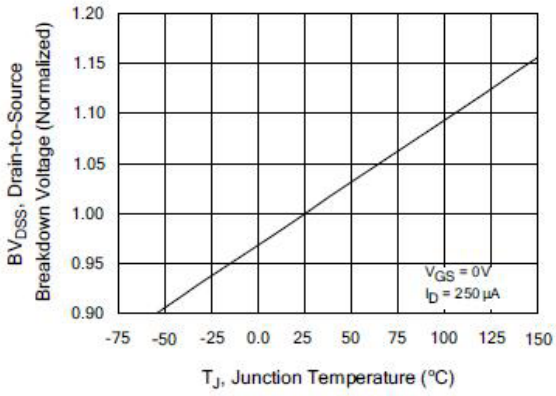


Figure 12. Typical Threshold Voltage vs Junction Temperature

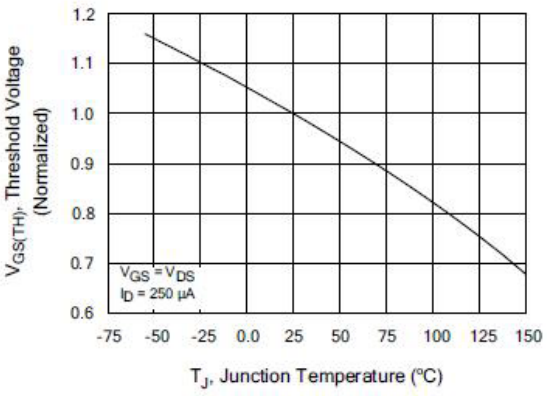


Figure 13. Maximum Forward Bias Safe Operating Area

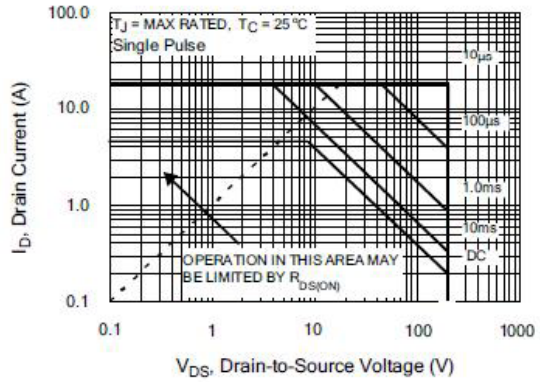


Figure 14. Typical Capacitance vs Drain-to-Source Voltage

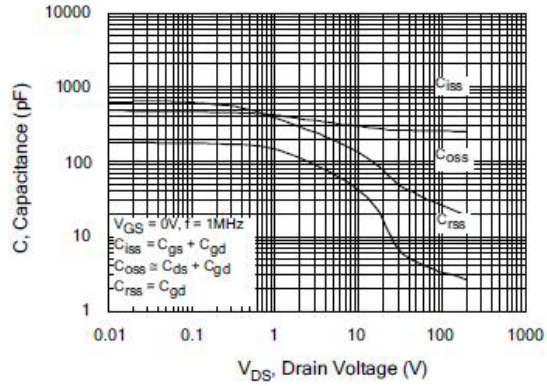


Figure 15. Typical Gate Charge vs Gate-to-Source Voltage

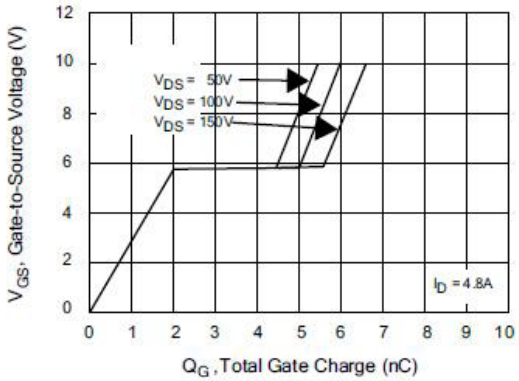


Figure 16. Typical Body Diode Transfer Characteristics