

Silicon N-Channel Power MOSFET

General Description :

HME3N150, the silicon N-channel Enhanced VDMOSFET, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-3PH, which accords with the RoHS standard.

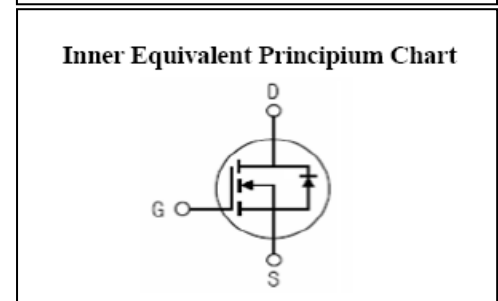
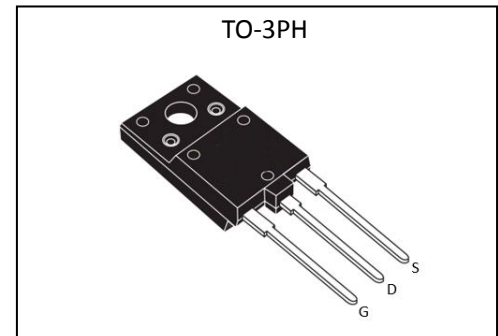
Features :

- Fast Switching
- Low ON Resistance
- Low Gate Charge Minimize Switching loss
- Fast Recovery Body Diode
- 100% Single Pulse avalanche energy Test

Applications :

- Adaptor
- Charger
- SMPS Standby Power

V_{DSS}	1500	V
I_D	3	A
$P_D(T_C=25^\circ\text{C})$	50	W
$R_{DS(ON)max}$	6.5	Ω



Absolute ($T_c = 25^\circ\text{C}$ unless otherwise specified) :

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	1500	V
I_D	Continuous Drain Current	3	A
I_{DM}	Pulsed Drain Current at $V_{GS}=10V$	12	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy	130	mJ
dv/dt	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation	50	W
	Derating Factor above 25°C	0.4	W/ $^\circ\text{C}$
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, -55 to 150	$^\circ\text{C}$
T_L	Maximum Temperature for Soldering	300	$^\circ\text{C}$
T_{PAK}	Leads at 0.63 in(1.6mm) from Case for 10 seconds, Package Body for 10 seconds	260	$^\circ\text{C}$

Caution Stresses greater than those in the "Absolute Maximum Ratings" may cause permanent damage to the device

Thermal Characteristics

Symbol	Parameter	Rating	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.5	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	40	$^{\circ}\text{C}/\text{W}$

Electrical Characteristics ($T_c = 25^{\circ}\text{C}$ unless otherwise specified) :

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	1500	--	--	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS}=1500\text{V}, V_{GS}=0\text{V}, T_a=25^{\circ}\text{C}$	--	--	10	μA
		$V_{DS}=1200\text{V}, V_{GS}=0\text{V}, T_a=125^{\circ}\text{C}$	--	--	250	
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=+30\text{V}$	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=-30\text{V}$	--	--	-100	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	$V_{GS}=10\text{V}, I_D=1.5\text{A}$	--	--	6.5	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	2.5	--	4.5	V
g_{fs}	Forward Transconductance	$V_{DS}=20\text{V}, I_D=1.5\text{A}$	--	2.0	--	S

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=25\text{V}$ $f=1.0\text{MHz}$	--	1900	--	pF
C_{oss}	Output Capacitance		--	100	--	
C_{rss}	Reverse Transfer Capacitance		--	13	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	$I_D=3\text{A}, V_{DD}=750\text{V}$ $V_{GS}=10\text{V}, R_g=10\Omega$	--	33	--	ns
t_r	Rise Time		--	16	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	58	--	
t_f	Fall Time		--	28	--	
Q_g	Total Gate Charge	$I_D=3\text{A}, V_{DD}=750\text{V}$ $V_{GS}=10\text{V}$	--	9.5	--	nC
Q_{gs}	Gate to Source Charge		--	15	--	
Q_{gd}	Gate to Drain ("Miller") Charge		--	5.5	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_{SD}	Continuous Source Current (Body Diode)		--	--	3	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	12	A
V_{SD}	Diode Forward Voltage	$I_S=3A, V_{GS}=0V$	--	--	1.5	V
trr	Reverse Recovery Time	$I_S=3A, T_j=25^\circ C$	--	300	--	ns
Qrr	Reverse Recovery Charge	$di/dt=100A/\mu s, V_{GS}=0V$	--		--	nC
*Pulse width $t_p \leq 380\mu s, \delta \leq 2\%$						

Characteristics Curve :

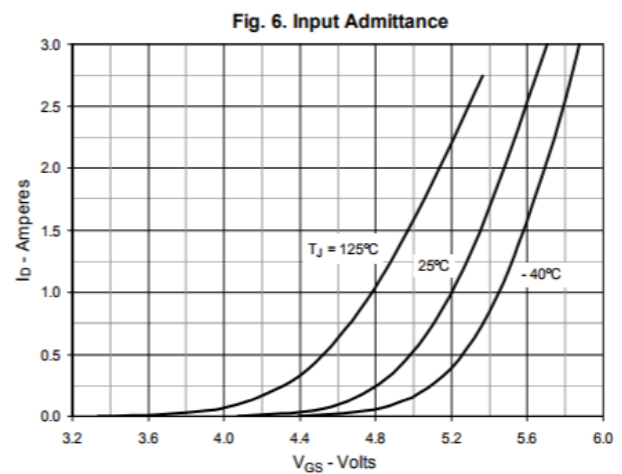
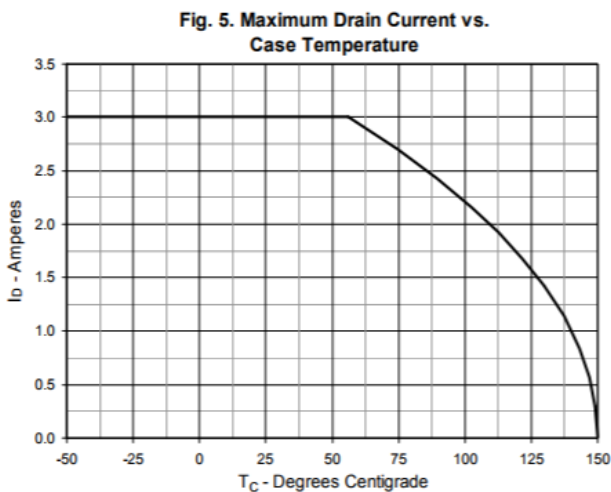
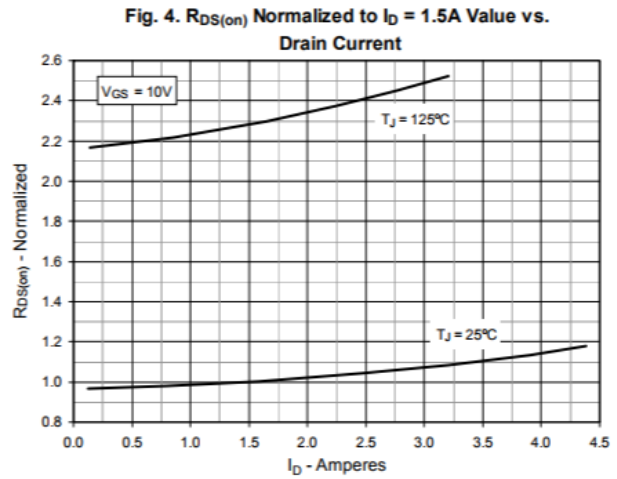
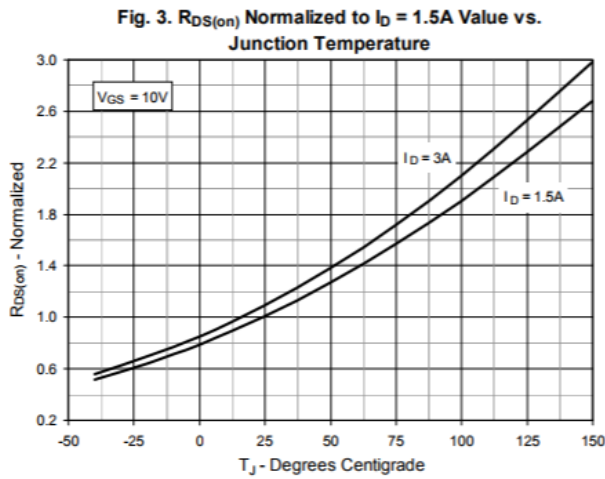
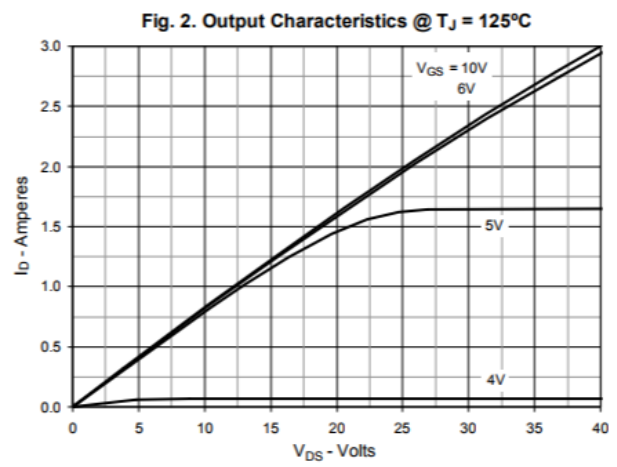
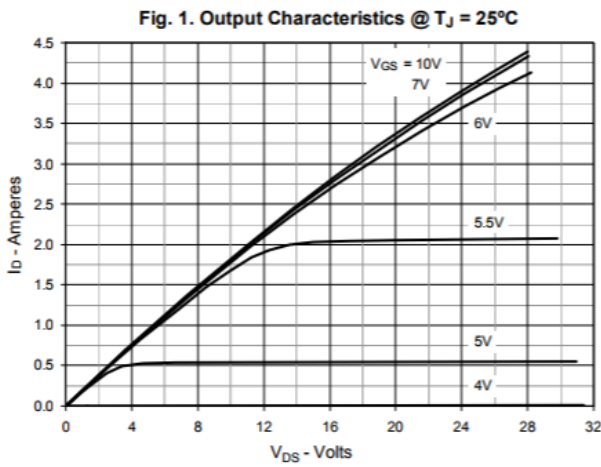


Fig. 7. Transconductance

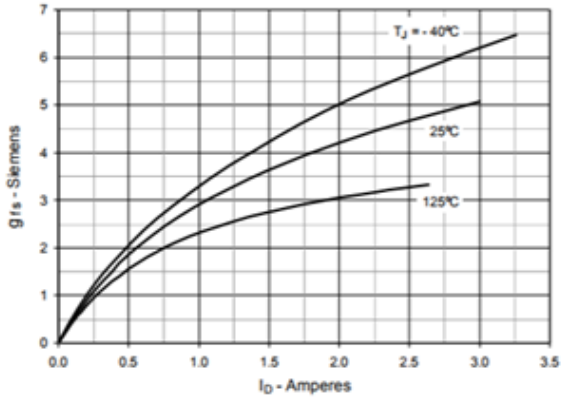


Fig. 8. Forward Voltage Drop of Intrinsic Diode

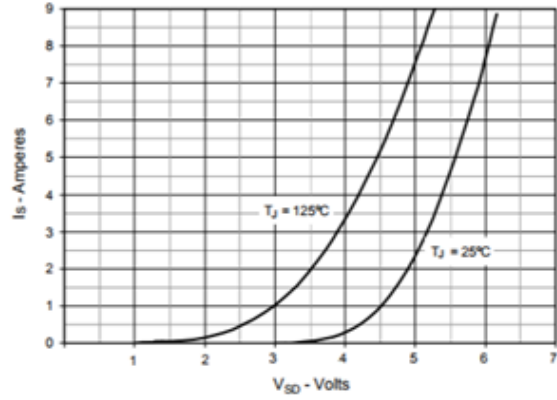


Fig. 9. Gate Charge

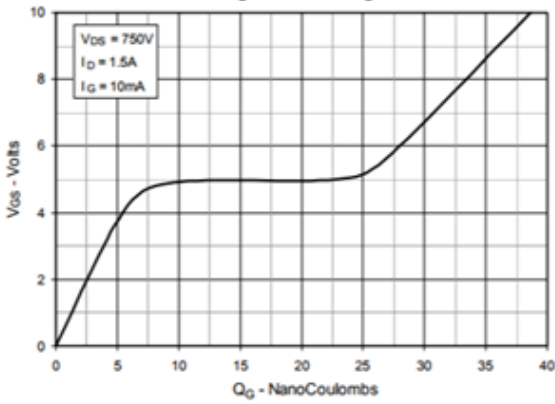


Fig. 10. Capacitance

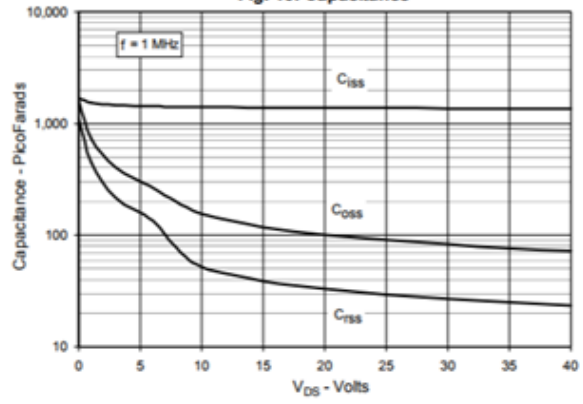


Fig. 11. Maximum Transient Thermal Impedance

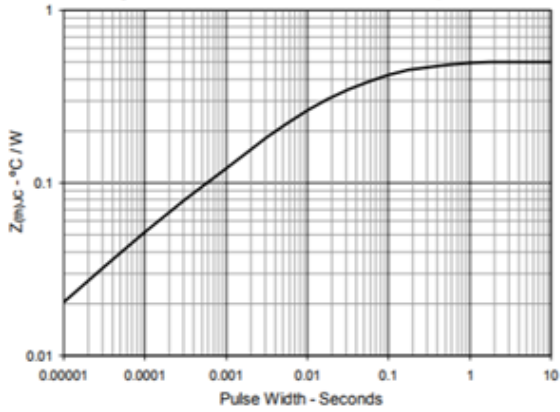


Fig. 12. Forward-Bias Safe Operating Area

