

Silicon N-Channel Power MOSFET

General Description :

HMT10N105, the silicon N-channel Enhanced VDMOSFET, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-3PN, which accords with the RoHS standard.

Features :

- Fast Switching
- Low ON Resistance($R_{dson} \leq 1.25\Omega$)
- Low Gate Charge
- Low Reverse transfer capacitances
- 100% Single Pulse avalanche energy Test

Applications:

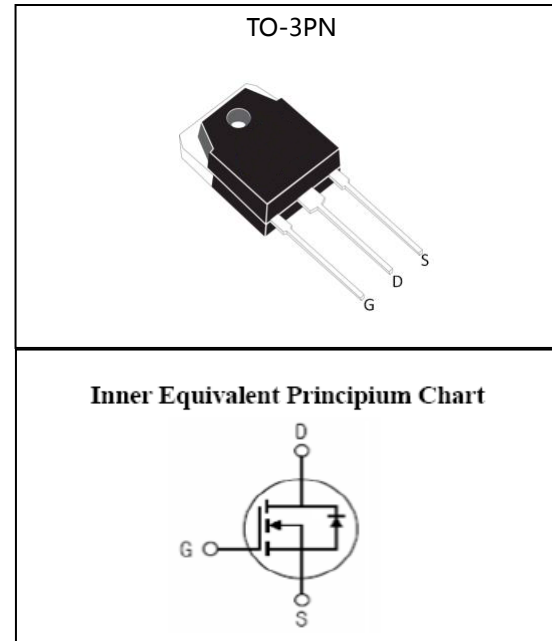
- Power switch circuit of adaptor and charger

Absolute ($T_c=25^\circ\text{C}$ unless otherwise specified) :

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	1050	V
I_D	Continuous Drain Current	10	A
I_{DM}^{a1}	Pulsed Drain Current	40	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}^{a2}	Single Pulse Avalanche Energy	900	mJ
dv/dt^{a3}	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation	50	W
	Derating Factor above 25°C	0.4	W/ $^\circ\text{C}$
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, -55 to 150	$^\circ\text{C}$
T_L	Maximum Temperature for Soldering	300	$^\circ\text{C}$

Caution Stresses greater than those in the "Absolute Maximum Ratings" may cause permanent damage to the device

V_{DSS}	1050	V
I_D	10	A
$P_D(T_C=25^\circ\text{C})$	300	W
$R_{DS(ON).TYP.}$	1.0	Ω



Thermal Characteristics

Symbol	Parameter	Rating	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.42	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	$^\circ\text{C}/\text{W}$

Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified) :

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	1050	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Bvdss Temperature Coefficient	$I_D=250\mu A, \text{Reference } 25^\circ\text{C}$	--	0.55	--	$V/^\circ\text{C}$
I_{DSS}	Drain to Source Leakage Current	$V_{DS}=1000V, V_{GS}=0V, T_a=25^\circ\text{C}$	--	--	1.0	μA
		$V_{DS}=900V, V_{GS}=0V, T_a=125^\circ\text{C}$	--	--	100	
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=+30V$	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=-30V$	--	--	-100	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	$V_{GS}=10V, I_D=5A$	--	1.0	1.25	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	--	4.0	V
g_{fs}	Forward Trans conductance	$V_{DS}=15V, I_D=5A$	--	7	--	S
Pulse width < 380 μ s; duty cycle < 2%.						

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	$V_{GS}=0V, V_{DS}=25V$ $f=1.0\text{MHz}$	--	2800	--	pF
C_{oss}	Output Capacitance		--	250	--	
C_{rss}	Reverse Transfer Capacitance		--	45	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	$I_D=10A, V_{DD}=500V$ $V_{GS}=10V, R_g=9.1\Omega$	--	45	--	ns
t_r	Rise Time		--	48	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	57	--	
t_f	Fall Time		--	52	--	
Q_g	Total Gate Charge	$I_D=10A, V_{DD}=500V$ $V_{GS}=10V$	--	72	--	nC
Q_{gs}	Gate to Source Charge		--	16	--	
Q_{gd}	Gate to Drain ("Miller") Charge		--	30	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_{SD}	Continuous Source Current (Body Diode)		--	--	10	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	40	A
V_{SD}	Diode Forward Voltage	$I_S=10A, V_{GS}=0V$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$I_S=10A, T_J=25^\circ C$	--	--	850	ns
Q_{rr}	Reverse Recovery Charge	$dI_F/dt=100A/\mu s, V_{GS}=0V$	--	--	4.4	μC

a1 : Repetitive rating; pulse width limited by maximum junction temperature

a2 : $L=10mH, I_D=18A, \text{Start } T_J=25^\circ C$

a3 : $I_{SD}=10A, di/dt \leq 100A/\mu s, V_{DD} \leq BV_{DS}, \text{Start } T_J=25^\circ C$

Fig. 1 Output Characteristics

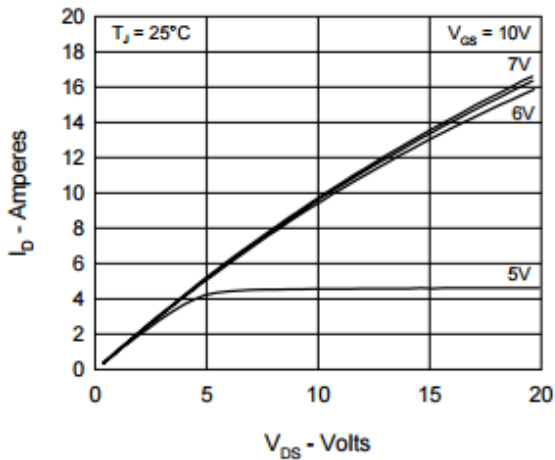


Fig. 2 Input Admittance

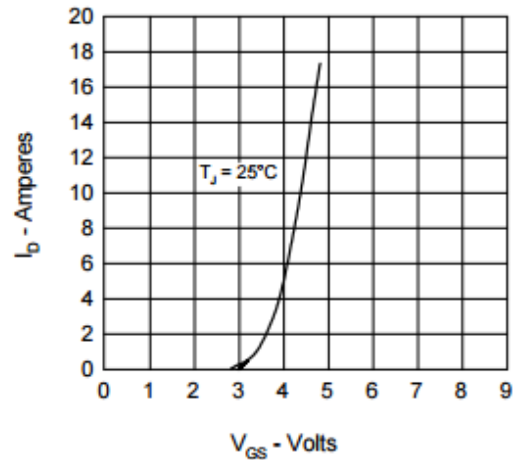


Fig. 3 $R_{DS(on)}$ vs. Drain Current

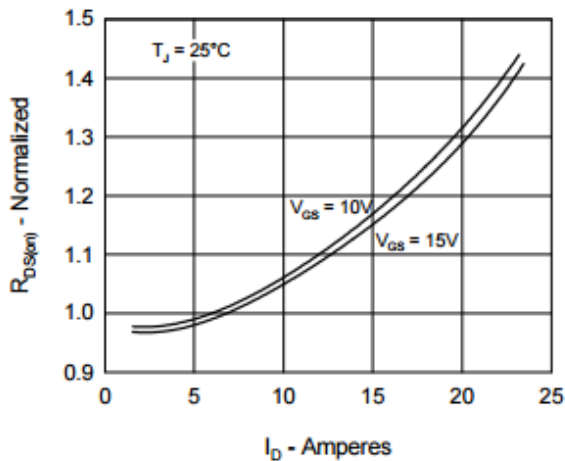


Fig. 4 Temperature Dependence of Drain to Source Resistance

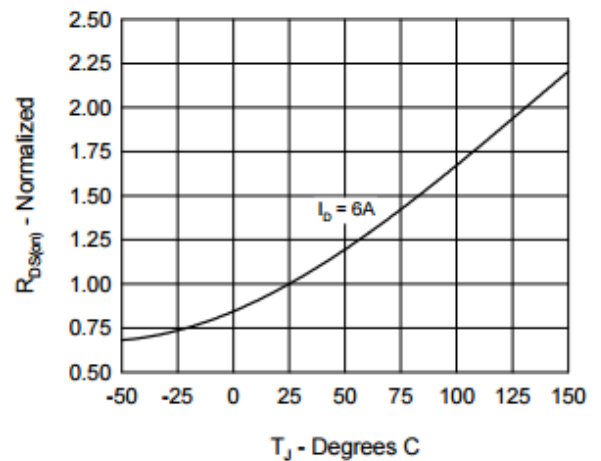


Fig. 5 Drain Current vs. Case Temperature

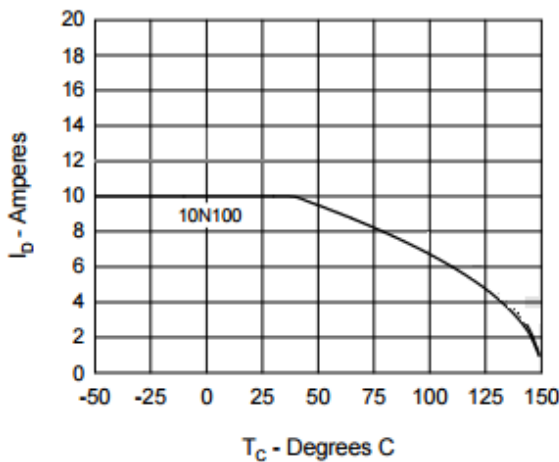


Fig. 6 Temperature Dependence of Breakdown and Threshold Voltage

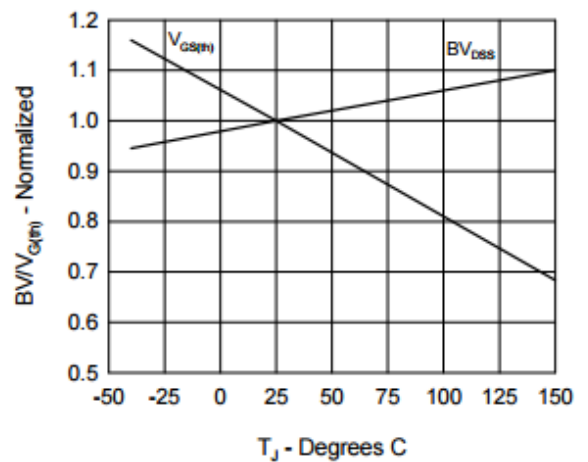


Fig.7 Gate Charge Characteristic Curve

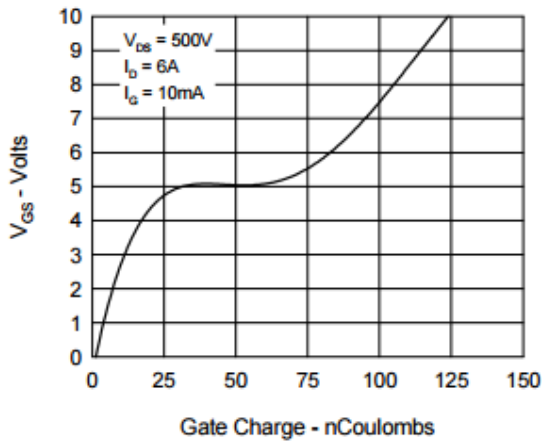


Fig.8 Forward Bias Safe Operating Area

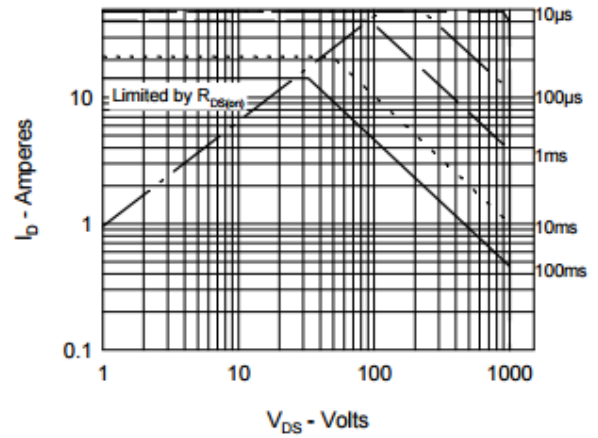


Fig.9 Capacitance Curves

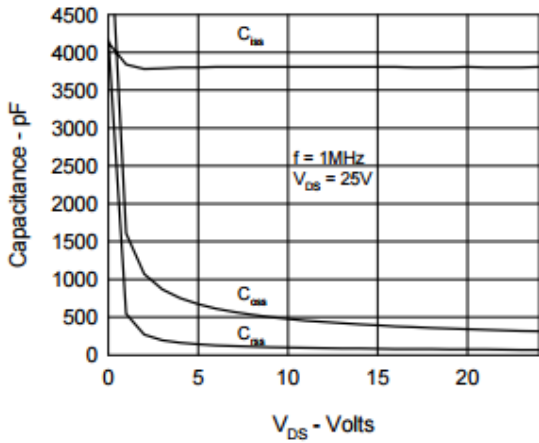


Fig.10 Source Current vs. Source to Drain Voltage

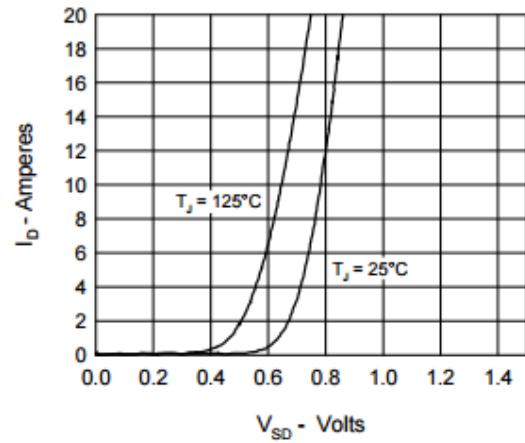


Fig.11 Transient Thermal Impedance

