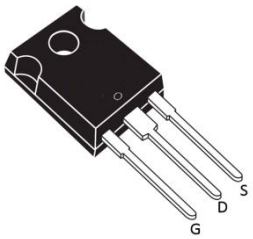
Silicon N-Channel Power MOSFET

General Description:

HMP15N50 the silicon N-channel Enhanced VDMOSFETS, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-247, which accords with the RoHS standard.

V_{DSS}	500	V
I_D	15	A
P_D (T_C=25℃)	180	W
$R_{DS(ON)typ}$	0.29	Ω

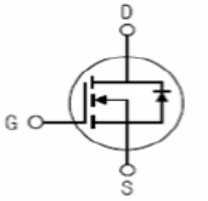
TO-247



Features:

- Fast Switching
- Low Gate Charge and Rdson
- Low Reverse transfer capacitances
- 100% Single Pulse avalanche energy Test

Inner Equivalent Principium Chart



Applications:

- Automotive、DC Motor Control and Class D Amplifier.

Absolute (Tc=25℃ unless otherwise specified):

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	500	V
I_D	Continuous Drain Current	15	A
	Continuous Drain Current T_C = 100 °C	9.5	A
I_{DM}[a1]	Pulsed Drain Current	60	A
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS} [a2]	Single Pulse Avalanche Energy	1000	mJ
E_{AR} [a1]	Avalanche Energy ,Repetitive	200	mJ
I_{AR} [a1]	Avalanche Current	6.3	A
dv/dt [a3]	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation	180	W
	Derating Factor above 25°C	1.44	W/℃
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, −55 to 150	℃
T_L	Maximum Temperature for Soldering	300	℃

Electrical Characteristics (Tc=25℃ unless otherwise specified):

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V,I_D=250μA	500	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Bvdss Temperature Coefficient	I_D=250uA,Reference25℃	--	0.60	--	V/℃
I_{DSS}	Drain to Source Leakage Current	V_{DS}=500V,V_{GS}=0V,T_a=25℃	--	--	1	μA
		V_{DS}=400V,V_{GS}=0V,T_a=125℃	--	--	250	
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS}=+30V	--	--	10	μA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS}=-30V	--	--	-10	μA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=7.5A	--	0.29	0.35	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	2.0	3.0	4.0	V
Pulse width tp≤380μs,δ≤2%						

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}	Forward Transconductance	V_{DS}=15V,I_D=7.5A	--	18	--	S
C_{iss}	Input Capacitance	V_{GS}=0V,V_{DS}= 25V f=1.0MHz	--	2400	--	pF
C_{oss}	Output Capacitance		--	240	--	
C_{rss}	Reverse Transfer Capacitance		--	25.5	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	I_D=15A,V_{DD} = 250V V_{GS}=10V,R_G=6.1Ω	--	15	--	ns
t_r	Rise Time		--	30	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	50	--	
t_f	Fall Time		--	40	--	
Q_g	Total Gate Charge	I_D=15A,V_{DD}=250V V_{GS}=10V	--	50	--	nC
Q_{gs}	Gate to Source Charge		--	12	--	
Q_{gd}	Gate to Drain (“Miller”)Charge		--	20	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)		--	--	15	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	60	A
V_{SD}	Diode Forward Voltage	I_S=15A,V_{GS}=0V	--	--	1.5	V
t_{rr}	Reverse Recovery Time	I_S=15A,T_j = 25°C	--	582	--	ns
Q_{rr}	Reverse Recovery Charge	dI_F/dt=100A/us,V_{GS}=0V	--	4.7	--	uC
Pulse width tp≤380μs,δ≤2%						

Symbol	Parameter	Typ.	Units
$R_{\theta JC}$	Junction-to-Case	0.68	℃/W
$R_{\theta JA}$	Junction-to-Ambient	40	℃/W

[a1]: Repetitive rating; pulse width limited by maximum junction temperature

[a2]: L=10.0mH, I_D=14A, Start T_J=25℃

[a3]: I_{SD} =15A,di/dt ≤100A/us,V_{DD}≤BV_{DS}, Start T_J=25℃

Test Circuit and Waveform

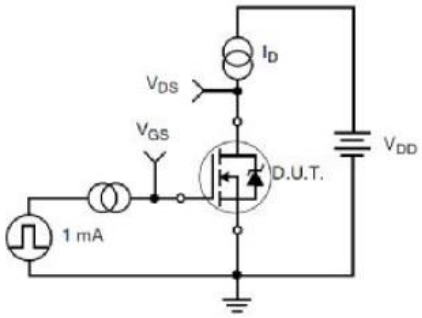


Figure 17. Gate Charge Test Circuit

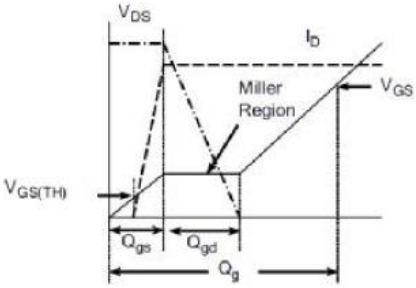


Figure 18. Gate Charge Waveform

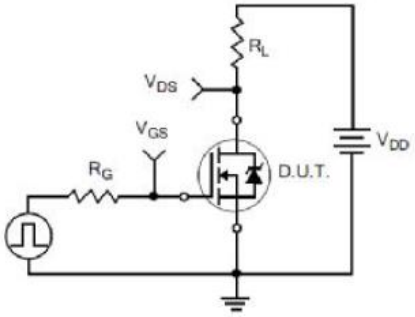


Figure 19. Resistive Switching Test Circuit

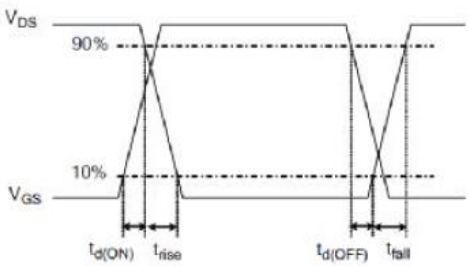


Figure 20. Resistive Switching Waveforms

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

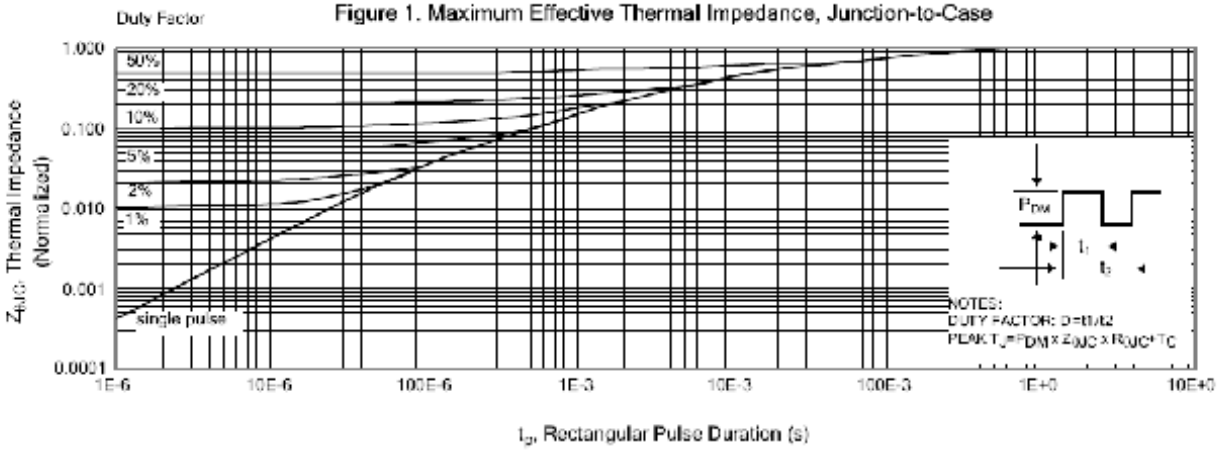


Figure 2. Maximum Power Dissipation vs Case Temperature

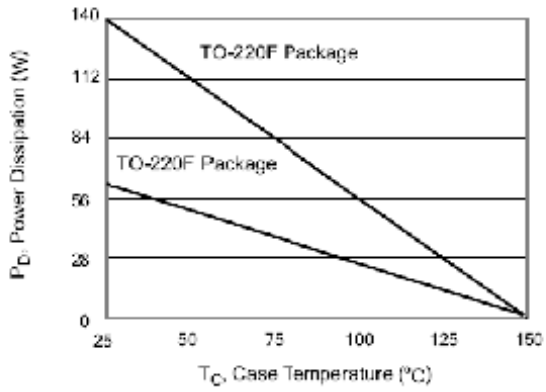


Figure 3. Maximum Continuous Drain Current vs Case Temperature

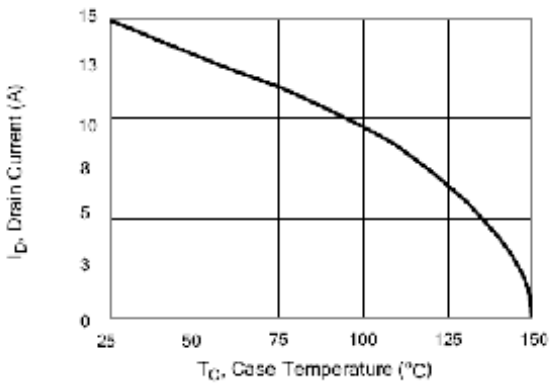


Figure 4. Typical Output Characteristics

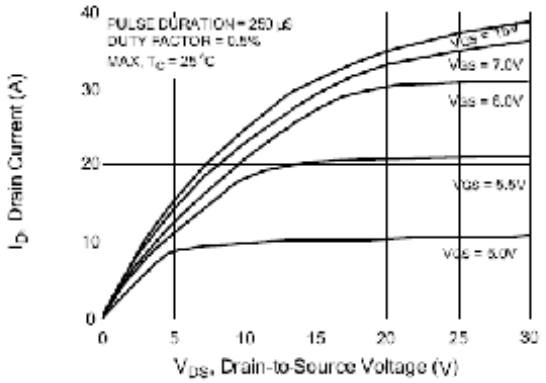


Figure 5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current

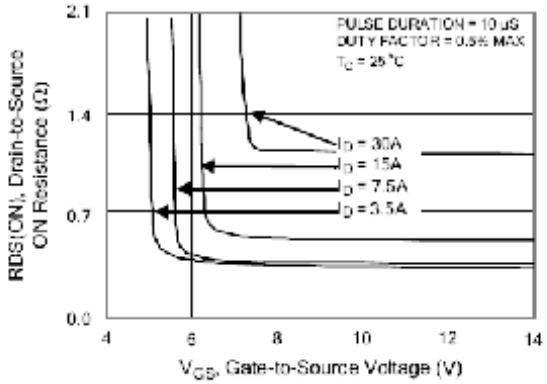


Figure 6. Maximum Peak Current Capability

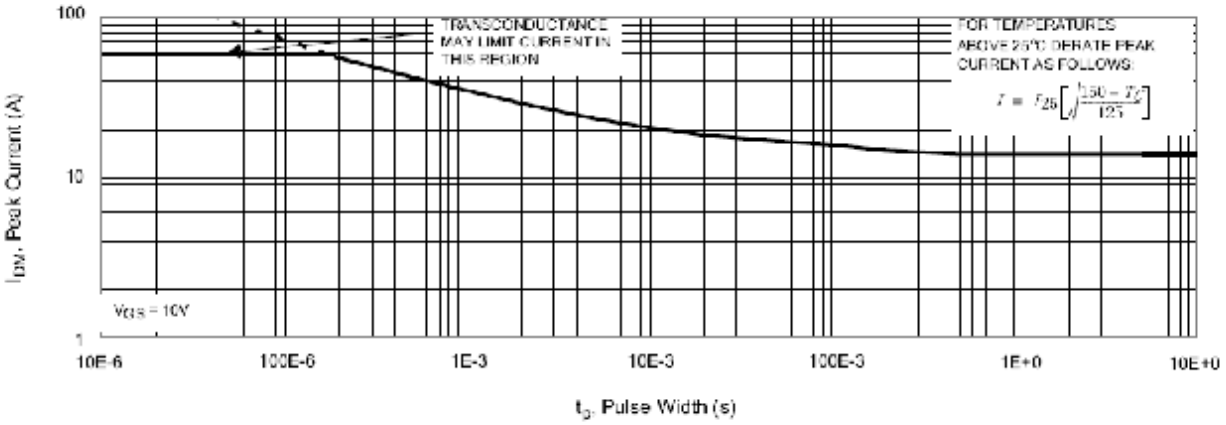


Figure 7. Typical Transfer Characteristics

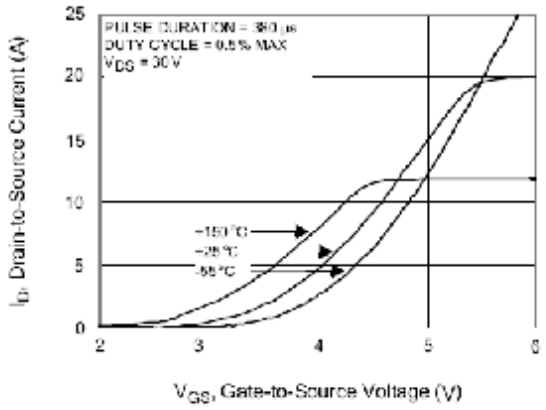


Figure 8. Unclamped Inductive Switching Capability

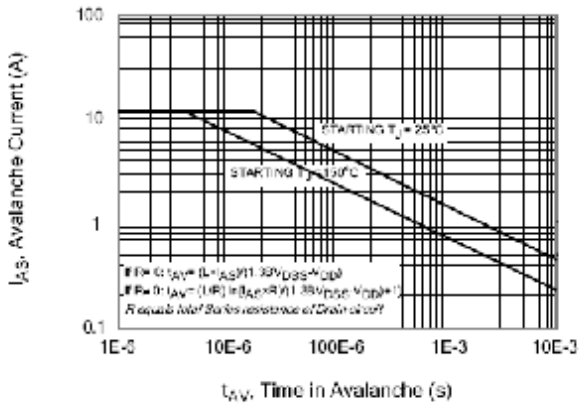


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

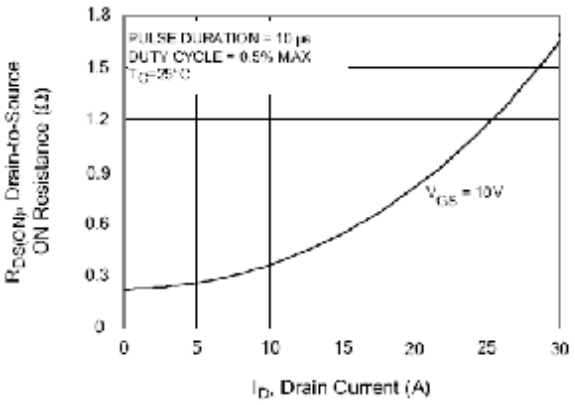


Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature

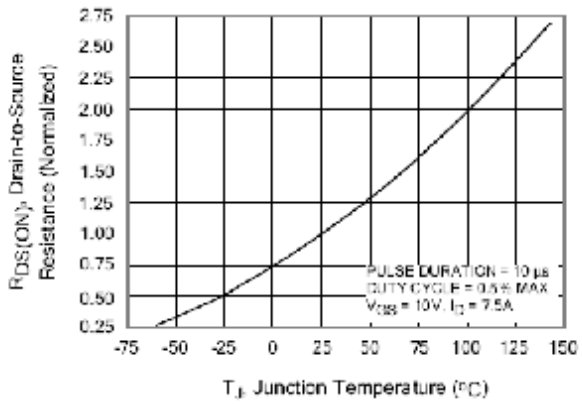


Figure 11. Typical Breakdown Voltage vs Junction Temperature

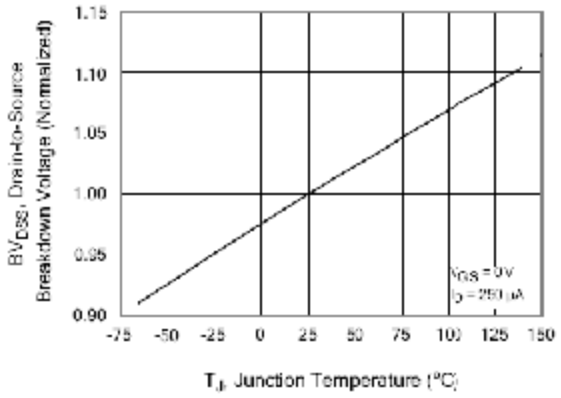


Figure 12. Typical Threshold Voltage vs Junction Temperature

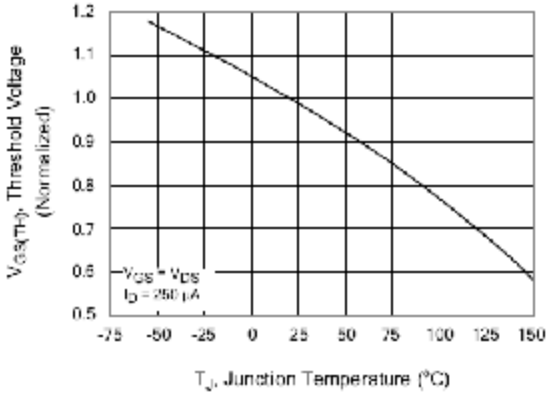


Figure 13. Maximum Forward Bias Safe Operating Area

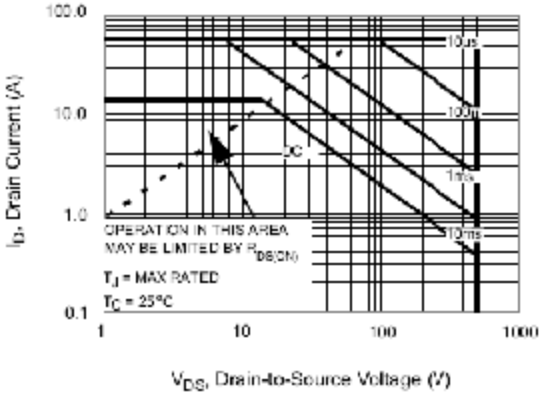


Figure 14. Typical Capacitance vs Drain-to-Source Voltage

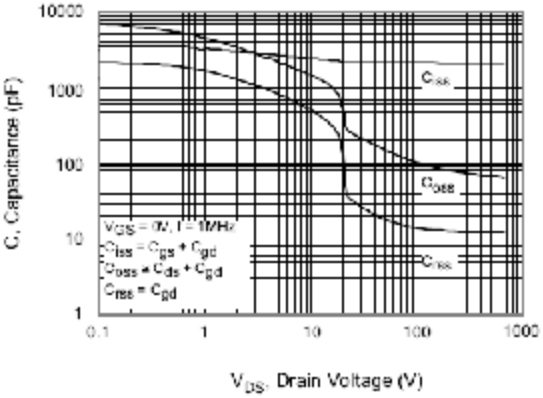


Figure 15. Typical Gate Charge vs Gate-to-Source Voltage

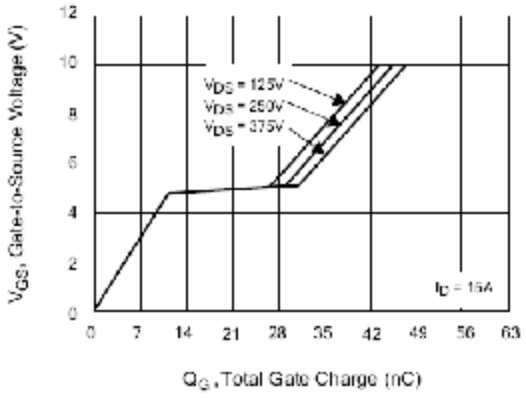
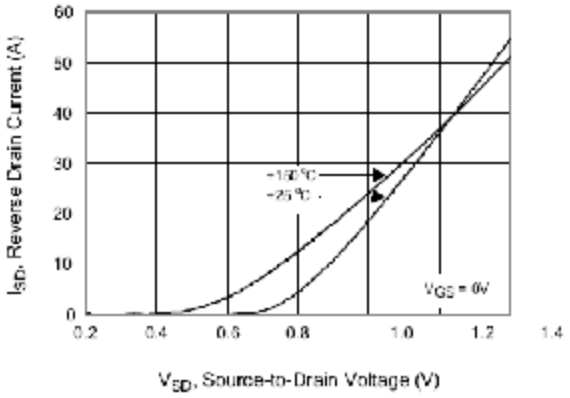


Figure 16. Typical Body Diode Transfer Characteristics



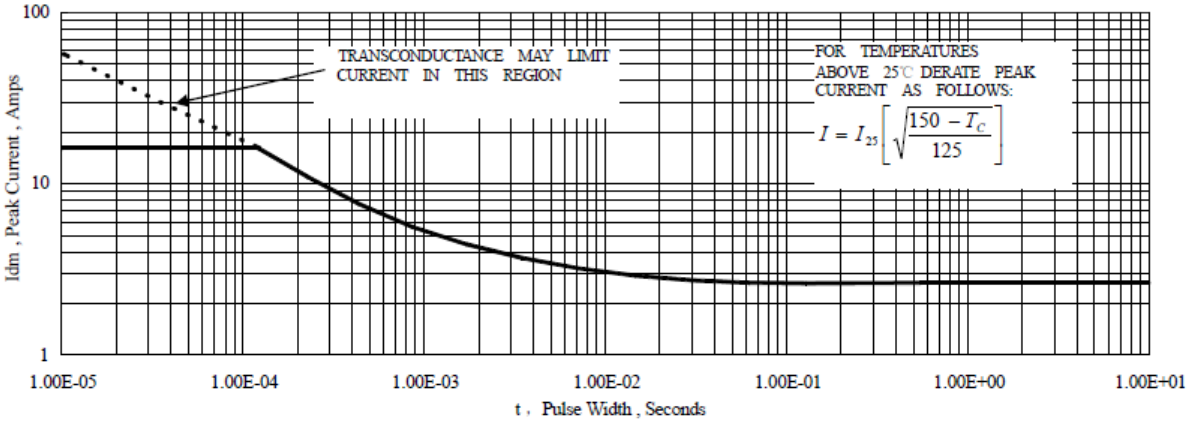


Figure 6 Maximum Peak Current Capability

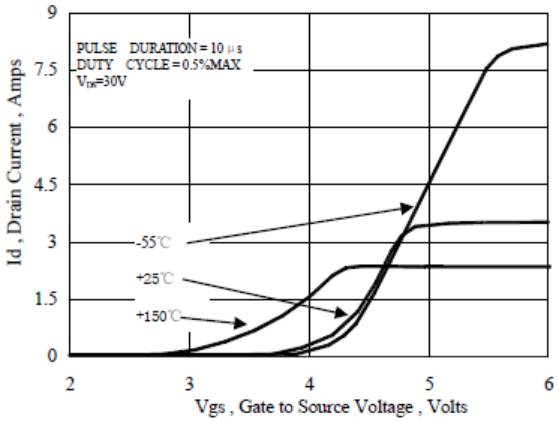


Figure 7 Typical Transfer Characteristics

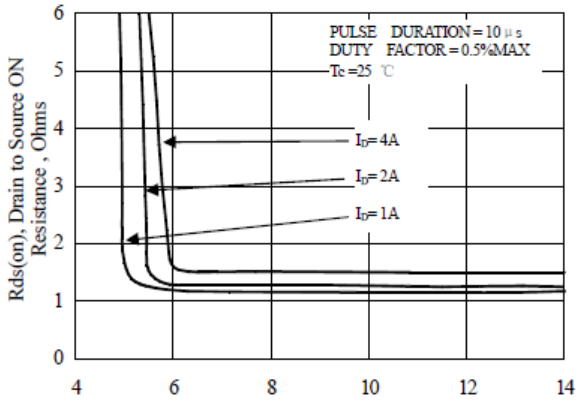


Figure 8 Typical Drain to Source ON Resistance vs Gate Voltage and Drain Current

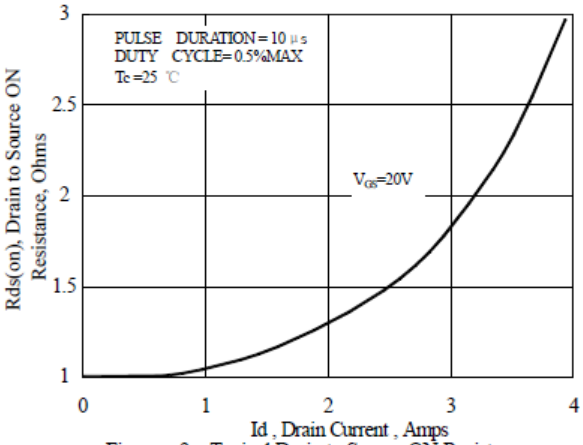


Figure 9 Typical Drain to Source ON Resistance vs Drain Current

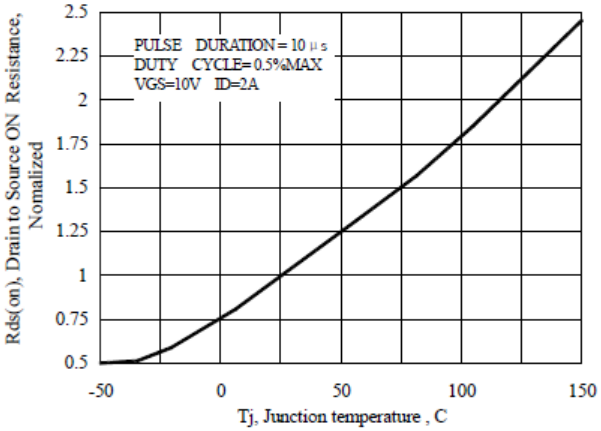


Figure 10 Typical Drian to Source on Resistance vs Junction Temperature