HMP3N150

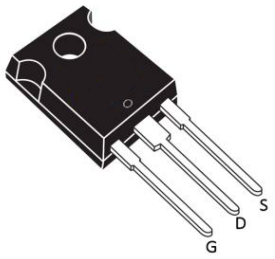
Silicon N-Channel Power MOSFET

General Description :

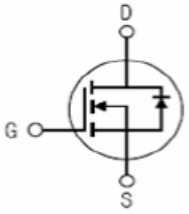
HMP3N150, the silicon N-channel Enhanced VDMOSFET, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-247, which accords with the RoHS standard.

V_{DSS}	1500	V
I_D	3	A
$P_D(T_C=25℃)$	250	W
$R_{DS(ON).type.}$	8	Ω

TO-247



Inner Equivalent Principium Chart



Features :

- Fast Switching
- Low ON Resistance
- Low Gate Charge Minimize Switching loss
- Fast Recovery Body Diode
- 100% Single Pulse avalanche energy Test

Applications :

- Adaptor
- Charger
- SMPS Standby Power

Absolute (Tc= 25℃ unless otherwise specified) :

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	1500	V
I_D	Continuous Drain Current	3	A
I_{DM}	Pulsed Drain Current at V_{GS}=10V	12	A
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy	130	mJ
dv/dt	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation	250	W
	Derating Factor above 25°C	2.0	W/℃
T_J,T_{stg}	Operating Junction and Storage Temperature Range	150,–55 to 150	℃
T_L T_{PAK}	Maximum Temperature for Soldering Leads at 0.63 in(1.6mm) from Case for 10 seconds, Package Body for 10 seconds	300 260	℃

Caution Stresses greater than those in the "Absolute Maximum Ratings" may cause permanent damage to the device

Thermal Characteristics

Symbol	Parameter	Rating	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.5	℃/ W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	50	℃/ W

Electrical Characteristics (Tc= 25℃ unless otherwise specified) :

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V,I_D=250μA	1500	--	--	V
I_{DSS}	Drain to Source Leakage Current	V_{DS}=1500V, V_{GS}=0V,T_a=25℃	--	--	10	μA
		V_{DS}=1200V, V_{GS}=0V,T_a=125℃	--	--	250	
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS}=+30V	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS}=-30V	--	--	-100	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=1.5A	--	8	10.5	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	2.5	--	4.5	V
g_{fs}	Forward Transconductance	V_{DS}=15V,I_D=10A	--	24	--	S

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	V_{GS}=0V V_{DS}=25V f=1.0MHz	--	1900	--	pF
C_{oss}	Output Capacitance		--	100	--	
C_{rss}	Reverse Transfer Capacitance		--	13	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	I_D=3A,V_{DD}=750V V_{GS}=10V,R_g=10Ω	--	33	--	ns
tr	Rise Time		--	16	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	58	--	
t_f	Fall Time		--	28	--	
Q_g	Total Gate Charge	I_D=3A,V_{DD}=750V V_{GS}=10V	--	9.5	--	nC
Q_{gs}	Gate to Source Charge		--	15	--	
Q_{gd}	Gate to Drain (“Miller”)Charge		--	5.5	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_{SD}	Continuous Source Current (Body Diode)		--	--	3	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	12	A
V_{SD}	Diode Forward Voltage	I_S=3A,V_{GS}=0V	--	--	5	V
trr	Reverse Recovery Time	I_S=3A,T_j=25℃	--	300	--	ns
Qrr	Reverse Recovery Charge	di/dt=100A/μs,V_{GS}=0V	--	--	--	nC
*Pulse width tp≤380μs,δ≤2%						

Characteristics Curve :

Fig. 1. Output Characteristics @ T_J = 25°C

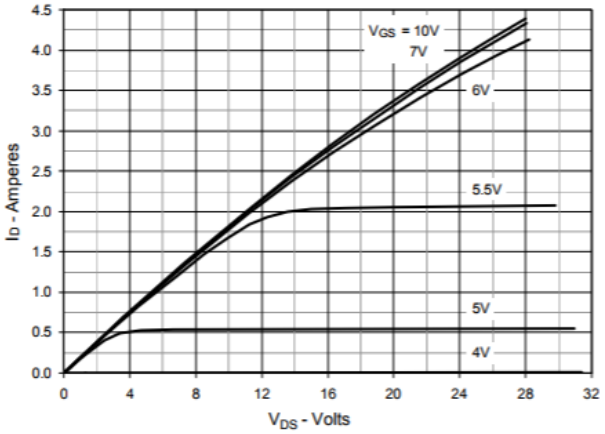


Fig. 2. Output Characteristics @ T_J = 125°C

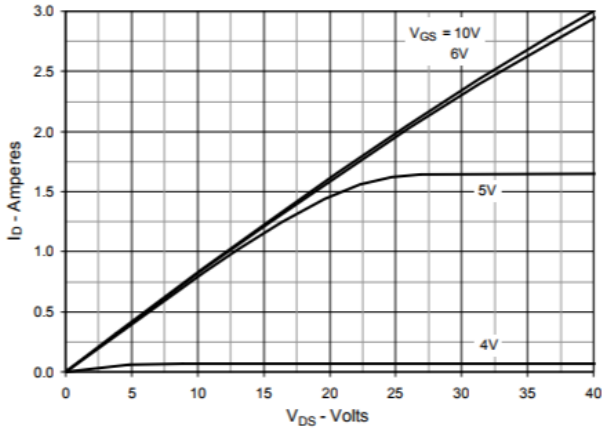


Fig. 3. $R_{DS(on)}$ Normalized to I_D = 1.5A Value vs. Junction Temperature

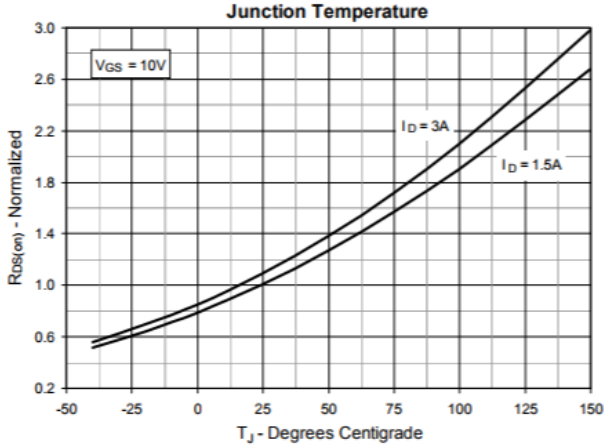


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 1.5A Value vs. Drain Current

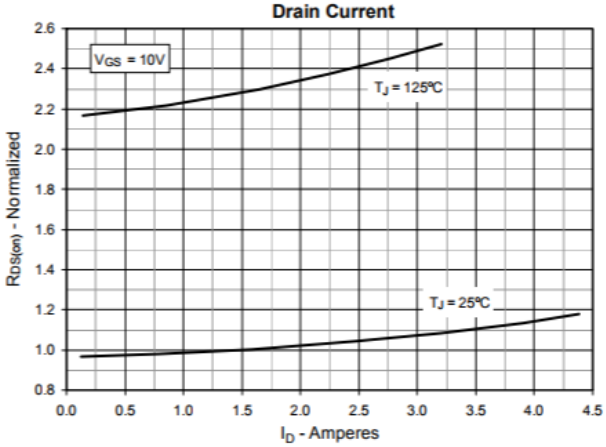


Fig. 5. Maximum Drain Current vs. Case Temperature

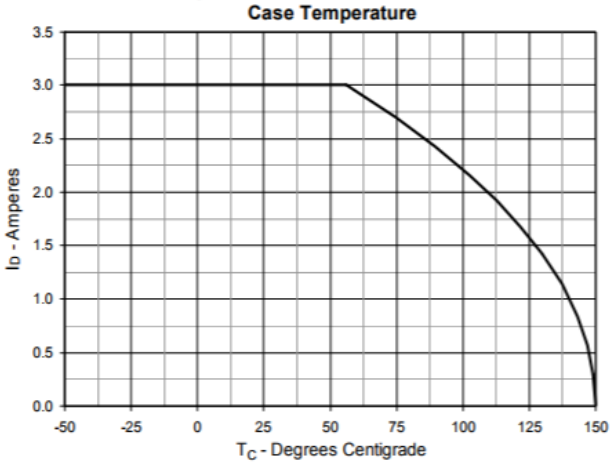


Fig. 6. Input Admittance

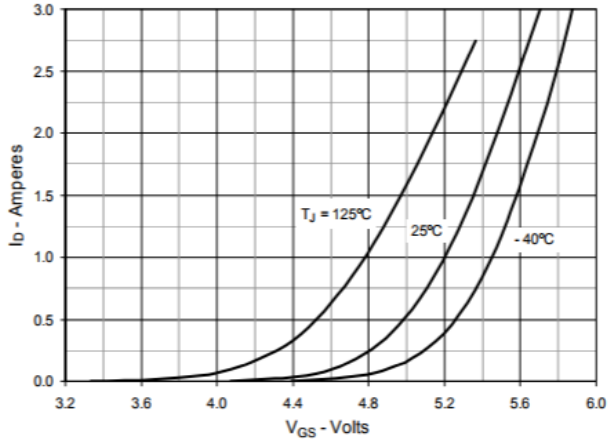


Fig. 7. Transconductance

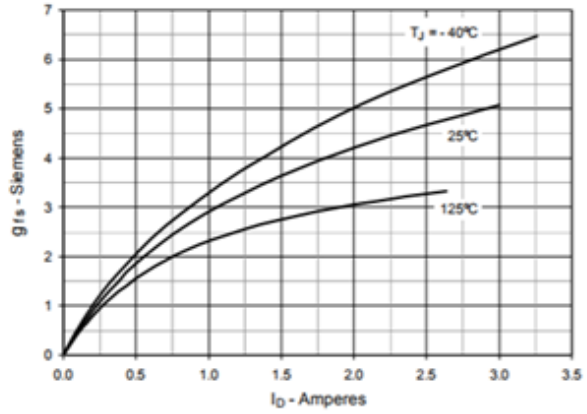


Fig. 8. Forward Voltage Drop of Intrinsic Diode

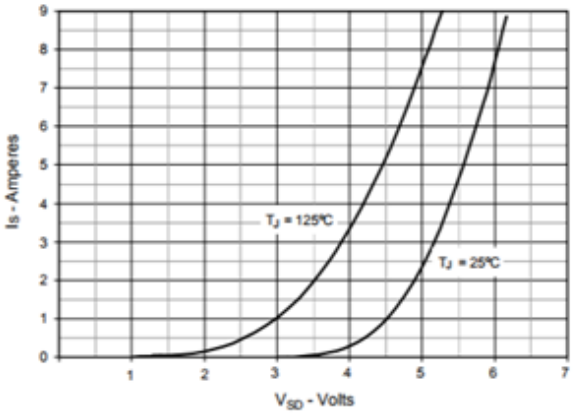


Fig. 9. Gate Charge

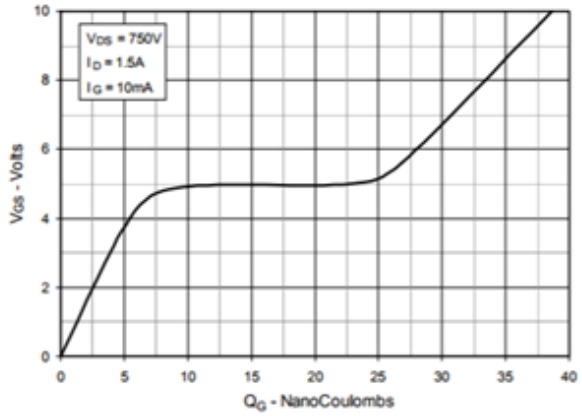


Fig. 10. Capacitance

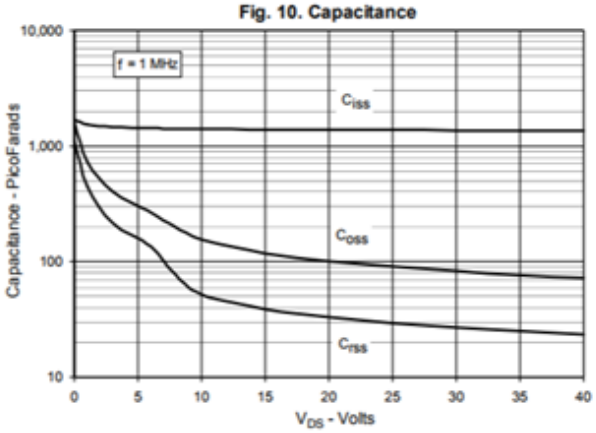


Fig. 11. Maximum Transient Thermal Impedance

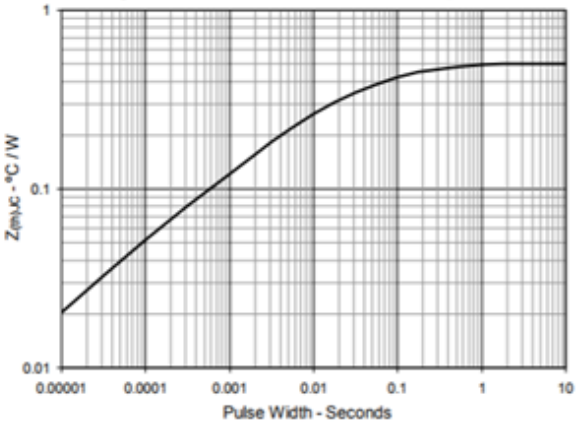


Fig. 12. Forward-Bias Safe Operating Area