HMM112N50

General Description:

HMM112N50 the silicon N-channel Enhanced VDMOSFETS, is obtained by the self-aligned plannr Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is SOT-227B, which accords with the RoHS standard.

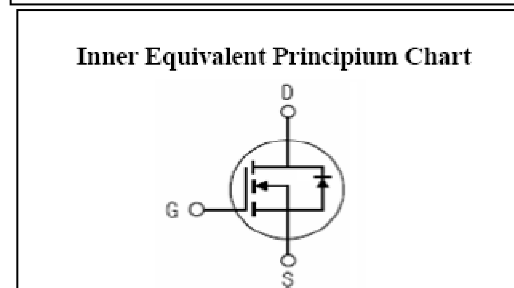
V_{DSS}	500	V
I_D	112	A
$P_D(T_C=25℃)$	1500	W
$R_{DS(ON)TYPE}$	38	mΩ

SOT-227B

Features:

- Fast Switching
- Low Gate Charge and R_{dson}
- Low Reverse transfer capacitances
- 100% Single Pulse avalanche energy Test

Inner Equivalent Principium Chart



Applications:

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply(UPS)
- Power Factor Correction(PFC)

Absolute (Tc=25℃ unless otherwise specified):

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	500	V
I_D	Continuous Drain Current	112	A
I_{DM} [a1]	Pulsed Drain Current (Pulse Width Limited by T_{JM})	330	A
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS} [a2]	Single Pulse Avalanche Energy	3.5	J
P_D	Power Dissipation	1500	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, –55 to 150	℃
T_L	MaximumTemperature for Soldering	300	℃

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	Typ.	Units
$R_{θJC}$	Junction-to-Case	0.083	℃/W

Electrical Characteristics（Tc=25℃ unless otherwise specified）:

OFF Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V,I_D=250μA	500	--	--	V
I_{DSS}	Drain to Source Leakage Current	V_{DS}=500V,V_{GS}=0V,T_a= 25℃	--	--	50	μA
		V_{DS}=400V,V_{GS}=0V,T_a=150℃	--	--	3000	
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS} =+30V	--	--	200	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS} =-30V	--	--	-200	nA

ON Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$[a3]	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=66A	--	38	50	mΩ
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	2.5	--	4.5	V

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}[a3]	Forward Transconductance	V_{DS}=10V, I_D=60A	--	100	--	S
C_{iss}	Input Capacitance	V_{GS}=0V,V_D=50V f=1.0MHz	--	16000	--	pF
C_{oss}	Output Capacitance		--	1410	--	
C_{rss}	Reverse Transfer Capacitance		--	88	--	

Resistive Switching Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	V_{DD}=250V,I_D=66A, V_{GS}=10V R_g=1.0Ω	--	48	--	ns
t_r	Rise Time		--	20	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	120	--	
t_f	Fall Time		--	17	--	
Q_g	Total Gate Charge	I_D =66A,V_{DD}=500V V_{GS}=0 to 10V	--	290	--	nC
Q_{gs}	Gate to Source Charge		--	70	--	
Q_{gd}	Gate to Drain（“Miller”）Charge		--	80	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)		--	--	112	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	330	A
V_{SD}	Diode Forward Voltage	I_S=100A,V_{GS}=0V	--	--	1.5	V
t_{rr}	Reverse Recovery Time	V_R=500V, V_{GS}=0V	--	130	250	ns
Q_{rr}	Reverse Recovery Charge	I_S=66A ,d_i/d_t=100A/us	--	560	--	nC
Pulse width tp≤380μs,δ≤2%						

a1: Repetitive rating; pulse width limited by maximum junction temperature

a2: I_{AS}=112A,V_{DD}=50V,R_G=1Ω, Starting T_J= 25°C

a3: Pulse Test: Pulse width≤380us, Duty Cycle≤2%

Fig. 1. Output Characteristics @ T_J = 25ºC

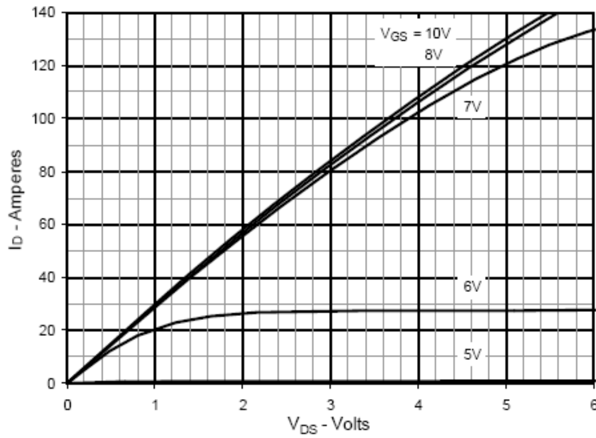


Fig. 2. Extended Output Characteristics @ T_J = 25ºC

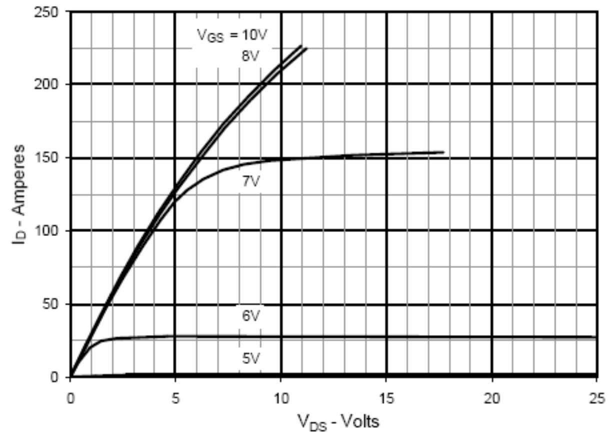


Fig. 3. Output Characteristics @ T_J = 125ºC

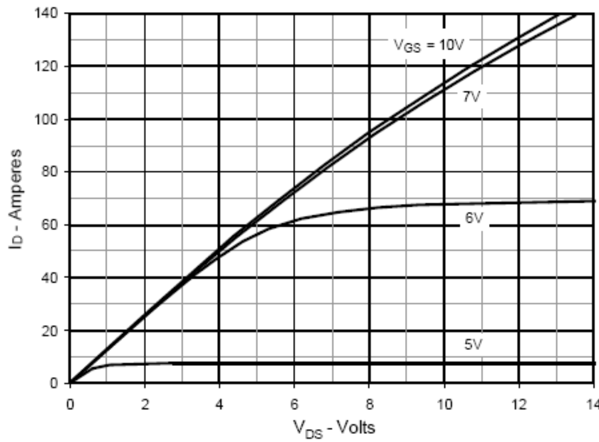


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 66A Value vs. Junction Temperature

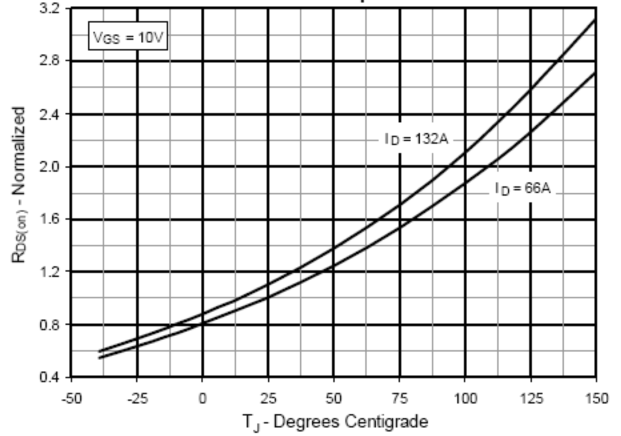


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 66A Value vs. Drain Current

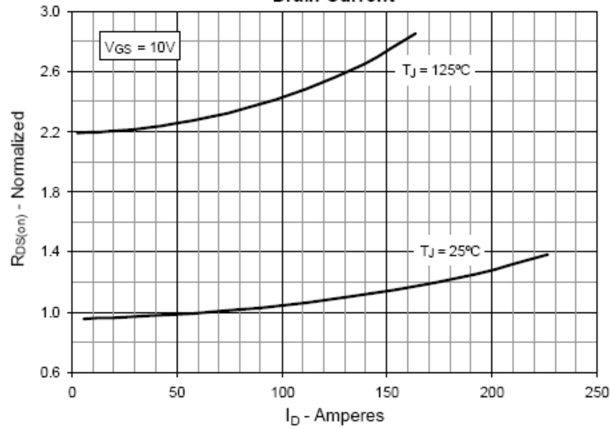
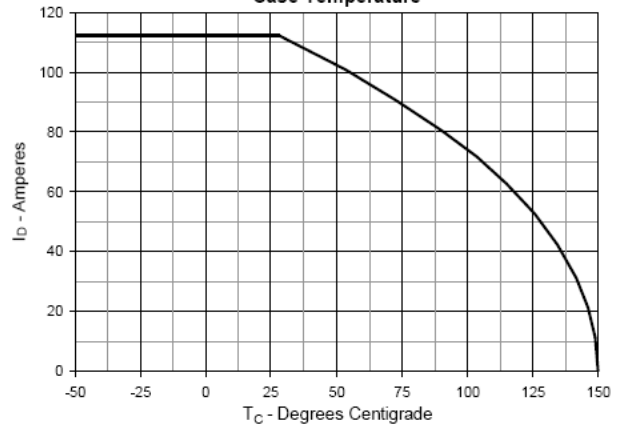


Fig. 6. Maximum Drain Current vs. Case Temperature



HSM

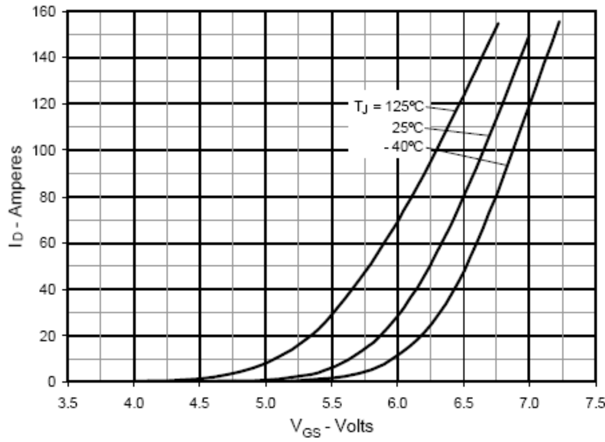


Fig. 7. Input Admittance
TJ = 125ºC
25ºC
- 40ºC
ID - Amperes
VGS - Volts

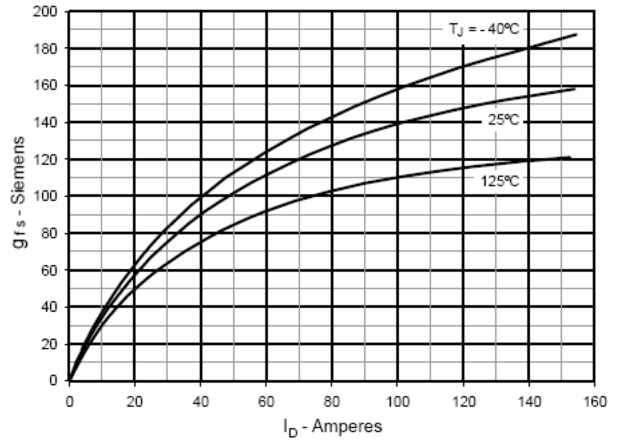


Fig. 8. Transconductance
TJ = - 40ºC
25ºC
125ºC
g f s - Siemens
ID - Amperes

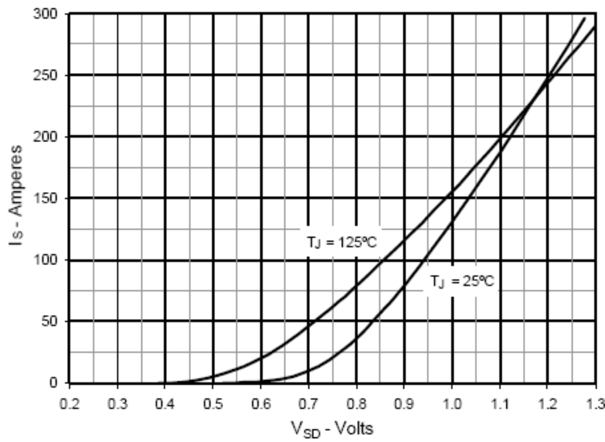


Fig. 9. Forward Voltage Drop of Intrinsic Diode
TJ = 125ºC
TJ = 25ºC
IS - Amperes
VSD - Volts

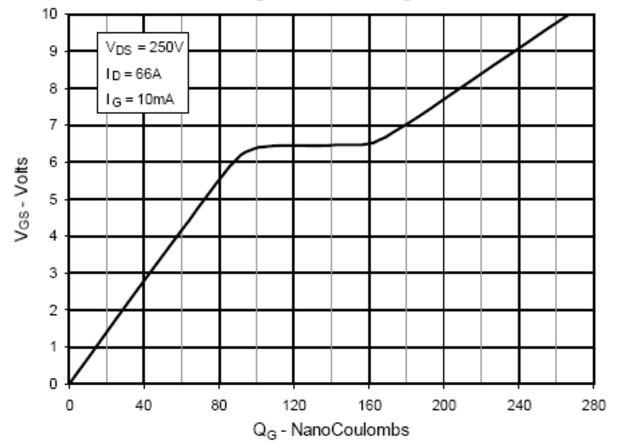


Fig. 10. Gate Charge
VDS = 250V
ID = 66A
IG = 10mA
VGS - Volts
QG - NanoCoulombs

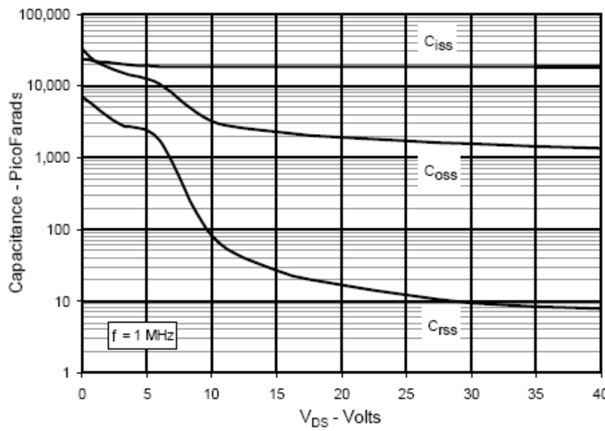


Fig. 11. Capacitance
Ciss
Coss
Crss
f = 1 MHz
Capacitance - PicoFarads
VDS - Volts

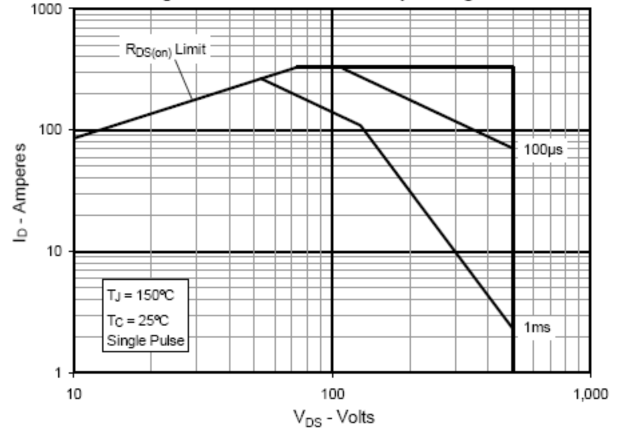


Fig. 12. Forward-Bias Safe Operating Area
RDS(on) Limit
100µs
1ms
TJ = 150ºC
TC = 25ºC
Single Pulse
ID - Amperes
VDS - Volts

Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

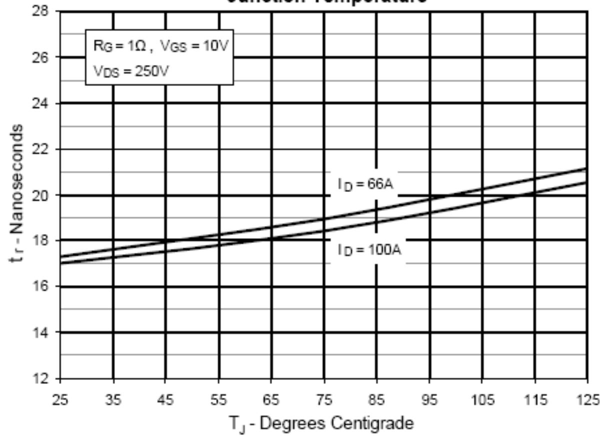


Fig. 14. Resistive Turn-on Rise Time vs. Drain Current

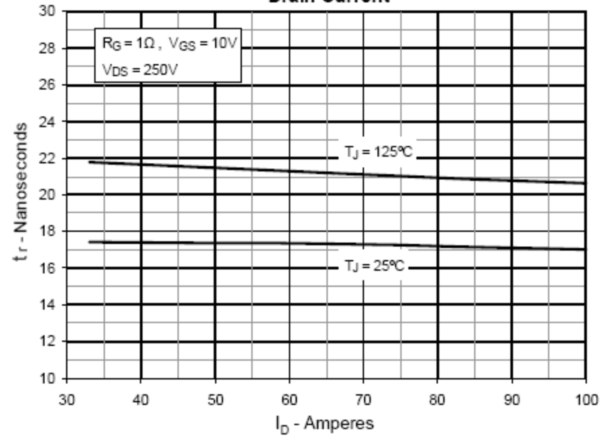


Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

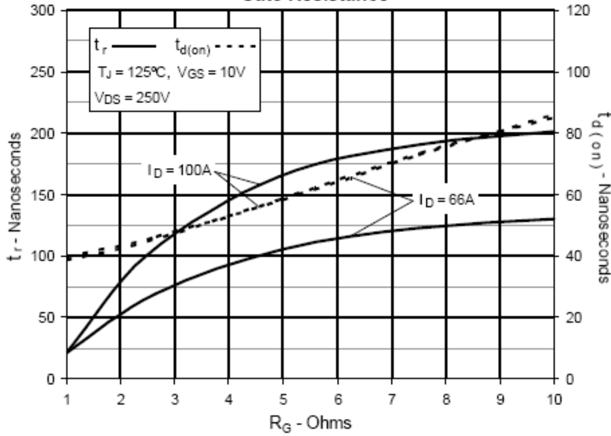


Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

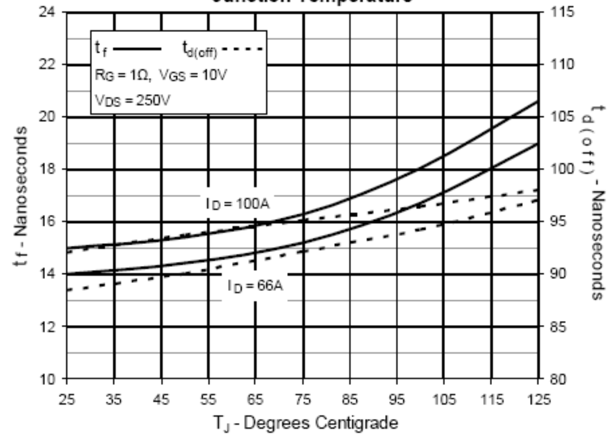


Fig. 17. Resistive Turn-off Switching Times vs. Drain Current

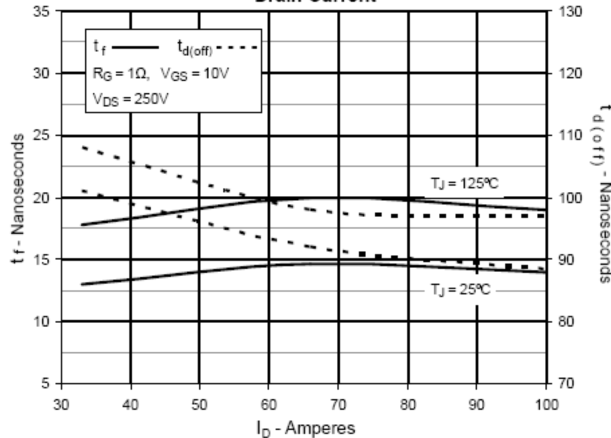
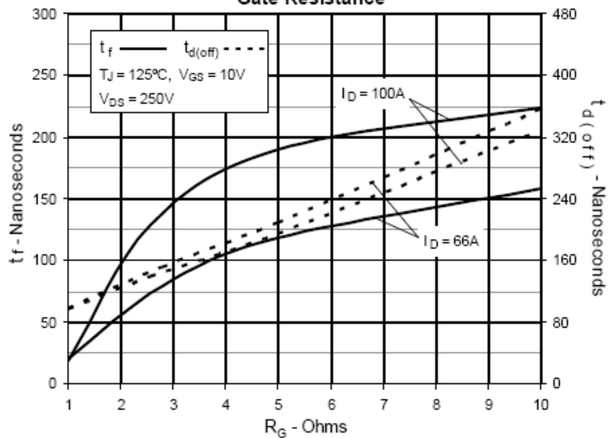


Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance



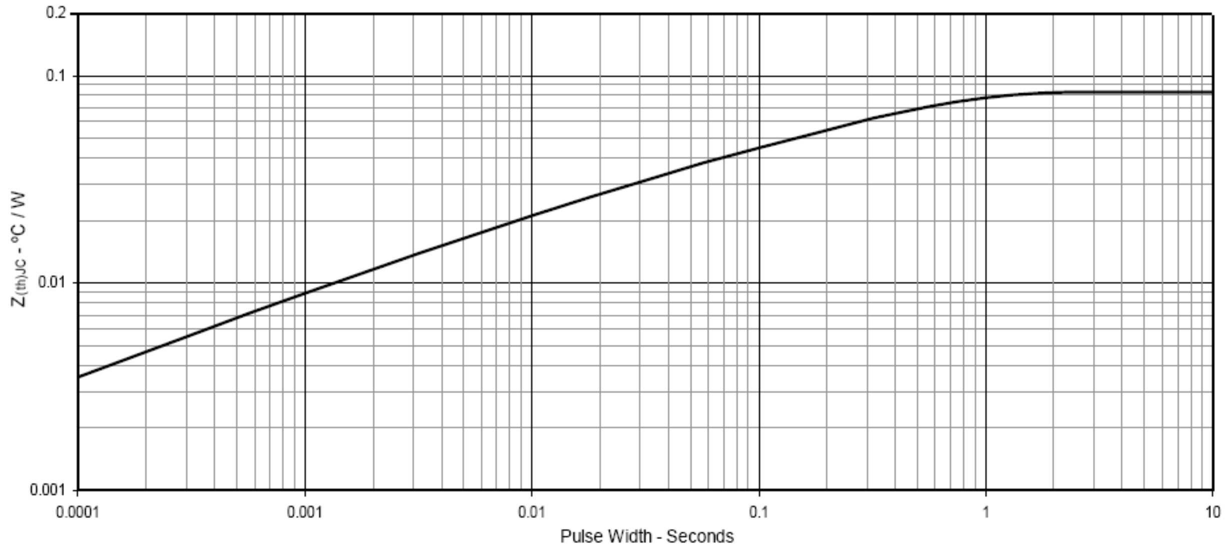


Fig. 19. Maximum Transient Thermal Impedance
0.2
0.1
0.01
0.001
Z(th)JC - ºC / W
0.0001
0.001
0.01
0.1
1
10
Pulse Width - Seconds