

General Description:

HSMM12R5N800, the silicon N-channel Enhanced VDMOSFET, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is Sot-227B, which accords with the RoHS standard..

$V_{DSS}(T_C=150^{\circ}C)$	800	V
I_D	62	A
$P_D(T_C=25^{\circ}C)$	700	W
$R_{DS(ON)TYPE}$	125	m Ω

SOT-227B



Features:

- Fast Switching
- ESD Improved Capability
- Low Gate Charge
- Low Reverse transfer capacitances
- 100% Single Pulse avalanche energy Test

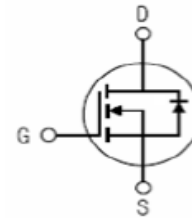
Applications:

- Power switch circuit of POWER

Absolute (Tc=25°C unless otherwise specified):

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	800	V
I_D	Continuous Drain Current	62	A
	Continuous Drain Current $T_C=100^{\circ}C$	41	A
I_{DM}^{a1}	Pulsed Drain Current(pulse width limited by T_{JM})	248	A
V_{GS}	Gate-to-Source Voltage	± 40	V
E_{AS}	Single Pulse Avalanche Energy	2000	mJ
E_{Ar}^{a1}	Avalanche Energy ,Repetitive	80	mJ
I_{AR}^{a1}	Avalanche Current	60	A
dv/dt^{a2}	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation	700	W
	Derating Factor above $25^{\circ}C$	5.6	W/ $^{\circ}C$
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, -55 to 150	$^{\circ}C$
T_L	Maximum Temperature for Soldering	300	$^{\circ}C$

Inner Equivalent Principium Chart



Thermal Characteristics

Symbol	Parameter	Rating	Units
R_{thJC}	Thermal Resistance, Junction-to-Case	0.179	°C/ W
R_{thcs}	Thermal Resistance, Case to heatsink	0.05	°C/ W

Electrical Characteristics (Tc= 25°C unless otherwise specified) :

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	800	--	--	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS}=800V, V_{GS}=0V, T_a=25^\circ C$	--	--	50	μA
		$V_{DS}=640V, V_{GS}=0V, T_a=125^\circ C$	--	--	3000	
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=+30V$	--	--	200	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=-30V$	--	--	-200	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	$V_{GS}=10V, I_D=31A$	--	--	145	m Ω
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=8mA$	3.0	--	6.0	V
g_{fs}	Forward Trans conductance	$V_{DS}=15V, I_D=31A$	--	33	--	S

Pulse width < 380 μ s; duty cycle < 2%.

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	$V_{GS}=0V, V_{DS}=25V$ $f=1.0MHz$	--	14000	--	PF
C_{oss}	Output Capacitance		--	1050	--	pF
C_{rss}	Reverse Transfer Capacitance		--	120	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	$I_D=20A, V_{DD}=400V$ $V_{GS}=10V, R_g=25\Omega$	--	55	--	ns
t_r	Rise Time		--	50	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	80	--	
t_f	Fall Time		--	45	--	
Q_g	Total Gate Charge	$I_D=40A, V_{DD}=400V$ $V_{GS}=10V$	--	260	--	nC
Q_{gs}	Gate to Source Charge		--	80	--	
Q_{gd}	Gate to Drain ("Miller") Charge		--	120	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_{SD}	Continuous Source Current (Body Diode)		--	--	62	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	248	A
V_{SD}	Diode Forward Voltage	$I_S=62A, V_{GS}=0V$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$I_S=62A, T_j=25^\circ C$	--	100	250	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt=100A/\mu s,$ $V_{GS}=0V$	--	2.5	--	μC

a1: Repetitive rating; pulse width limited by maximum junction temperature

a2: $I_{SD}=60A, di/dt \leq 100A/\mu s, V_{DD} \leq BV_{DS},$ Start $T_j=25^\circ C$

Characteristics Curve:

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

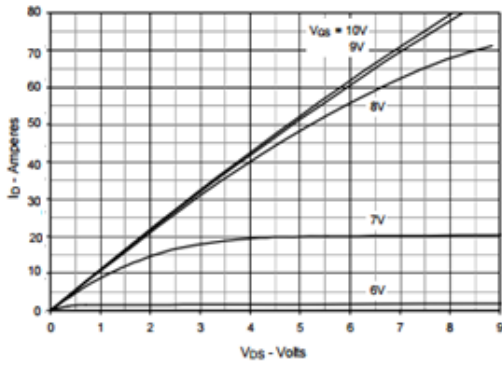


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

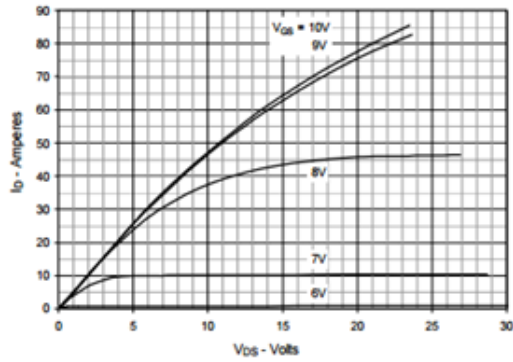


Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

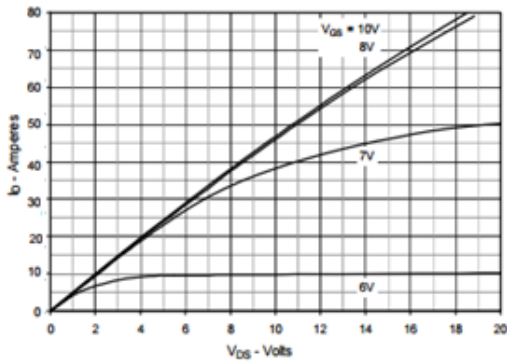


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 20\text{A}$ Value vs. Junction Temperature

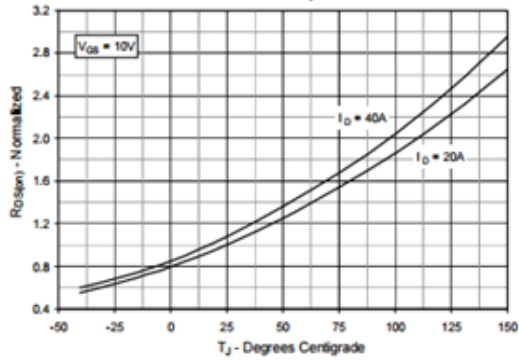


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 20\text{A}$ Value vs. Drain Current

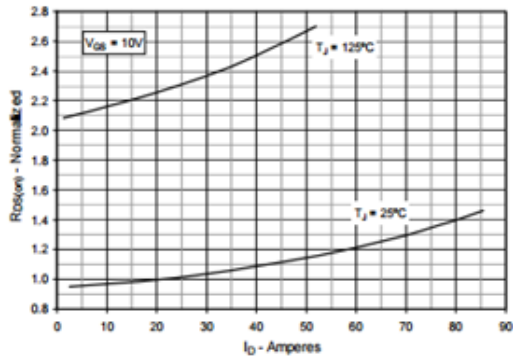
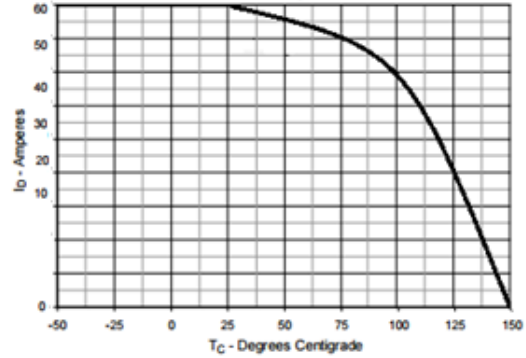


Fig. 6. Maximum Drain Current vs. Case Temperature





HSM12R5N800

Fig. 7. Input Admittance

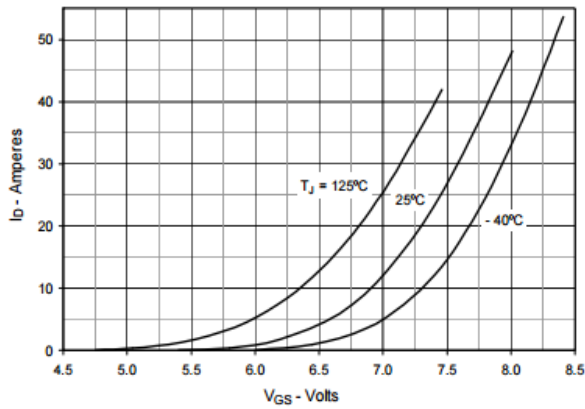


Fig. 8. Transconductance

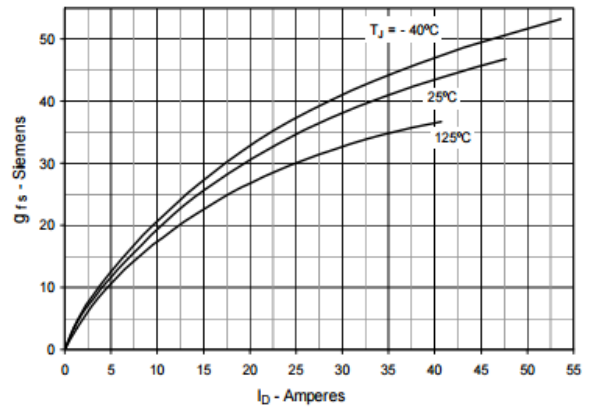


Fig. 9. Forward Voltage Drop of Intrinsic Diode

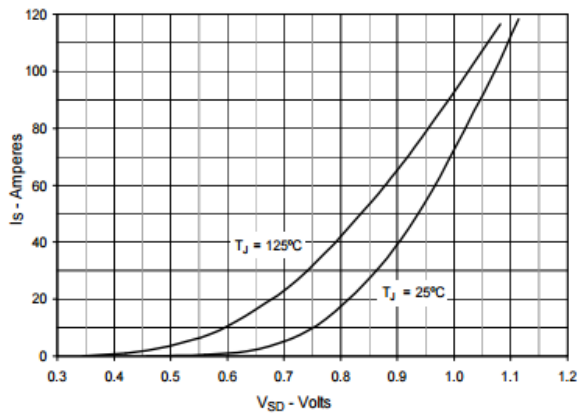


Fig. 10. Gate Charge

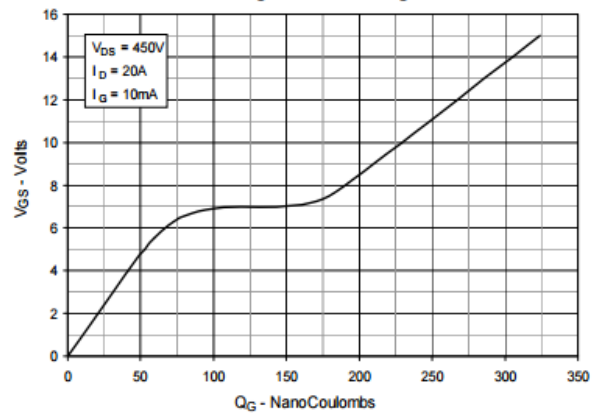


Fig. 11. Capacitance

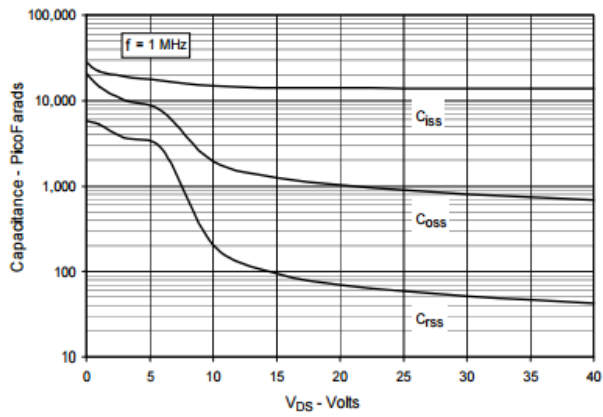


Fig. 12. Maximum Transient Thermal Impedance

